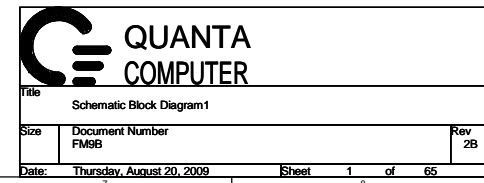


**PWB:**




## Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Clarksfield/Auburndale
7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	BLANK PAGE
23	HDMI CONN
24	LCD CONN
25	CRT CONN
26	R5U230
27	BLANK PAGE
28	Express/CRard/1394
29	SIO (ITE8502)
30	FLASH / RTC
31	MINI-Card (WWAN)
32	MINI-Card (WLAN/WPAN)
33	Left PUSB/ESATA
34	Right USB
35	SATA (HDD & CD-ROM)
36	TP / KEYBOARD
37	SWITCH / LED
38	FAN / THERMAL
39	Azelia CODEC
40	AUDIO CONN
41	LAN(RTL8111DL/RJ-45)
42	System Reset Circuit
43	Blank Page
44	1.8V_RUN(RT9018/RT9024)
45	Charger (MAX8731)
46	3V/5V (TPS51427A)
47	1.5_DDR/0.75(TPS51116)
48	1.05V_PCH(TPS51218)
49	1.05_VTT(TPS51218)
50	GFX_VCORE (MAX17028)
51	CPU CORE(MAX17036)
52	Run Power Switch
53	DCin & Batt
54	PAD & SCREW
55	EMI CAP
56	SMBUS BLOCK
57	THERMAL MAP
58	Power Block Diagram
59	Power sequence Block
60	XDP

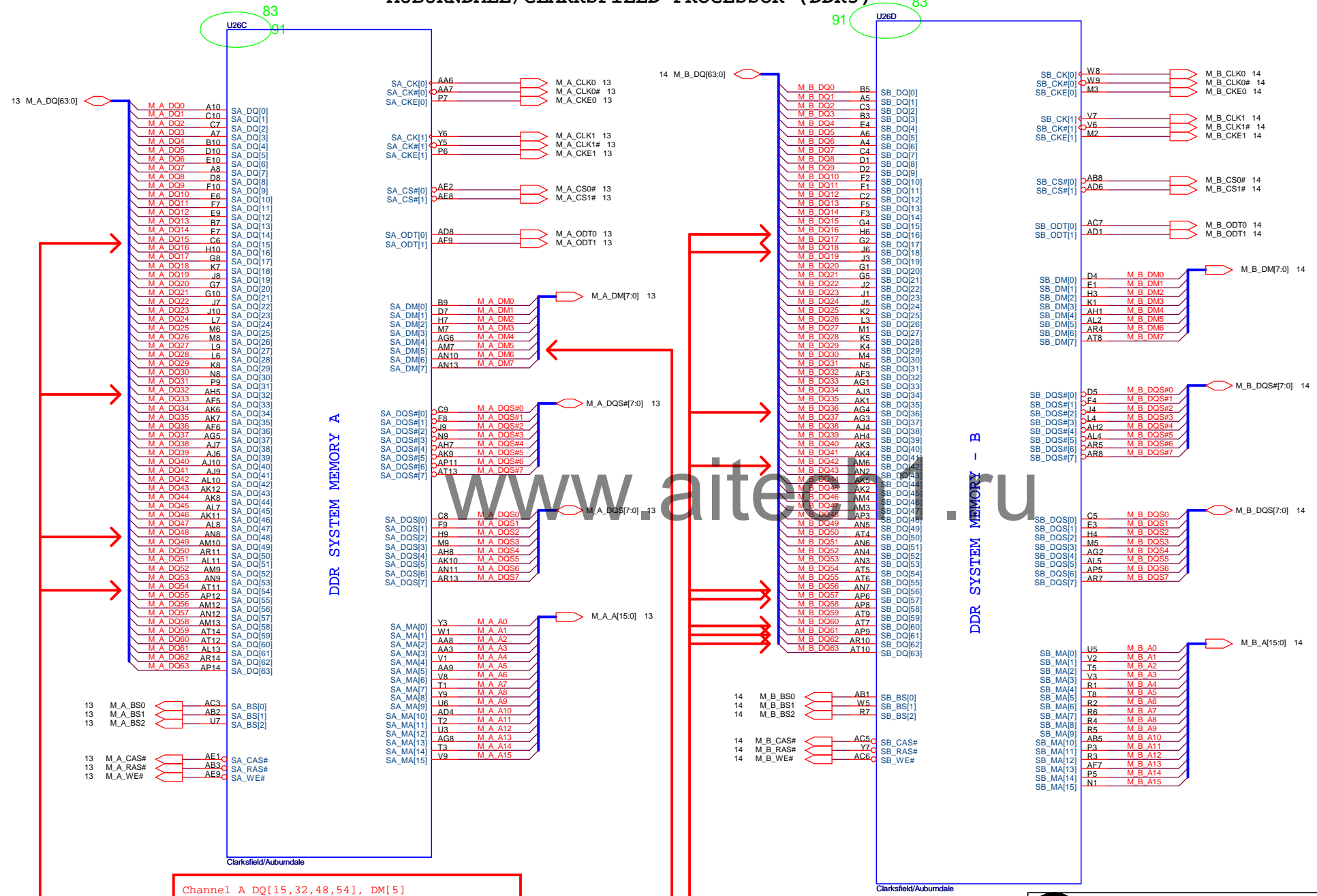
## Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



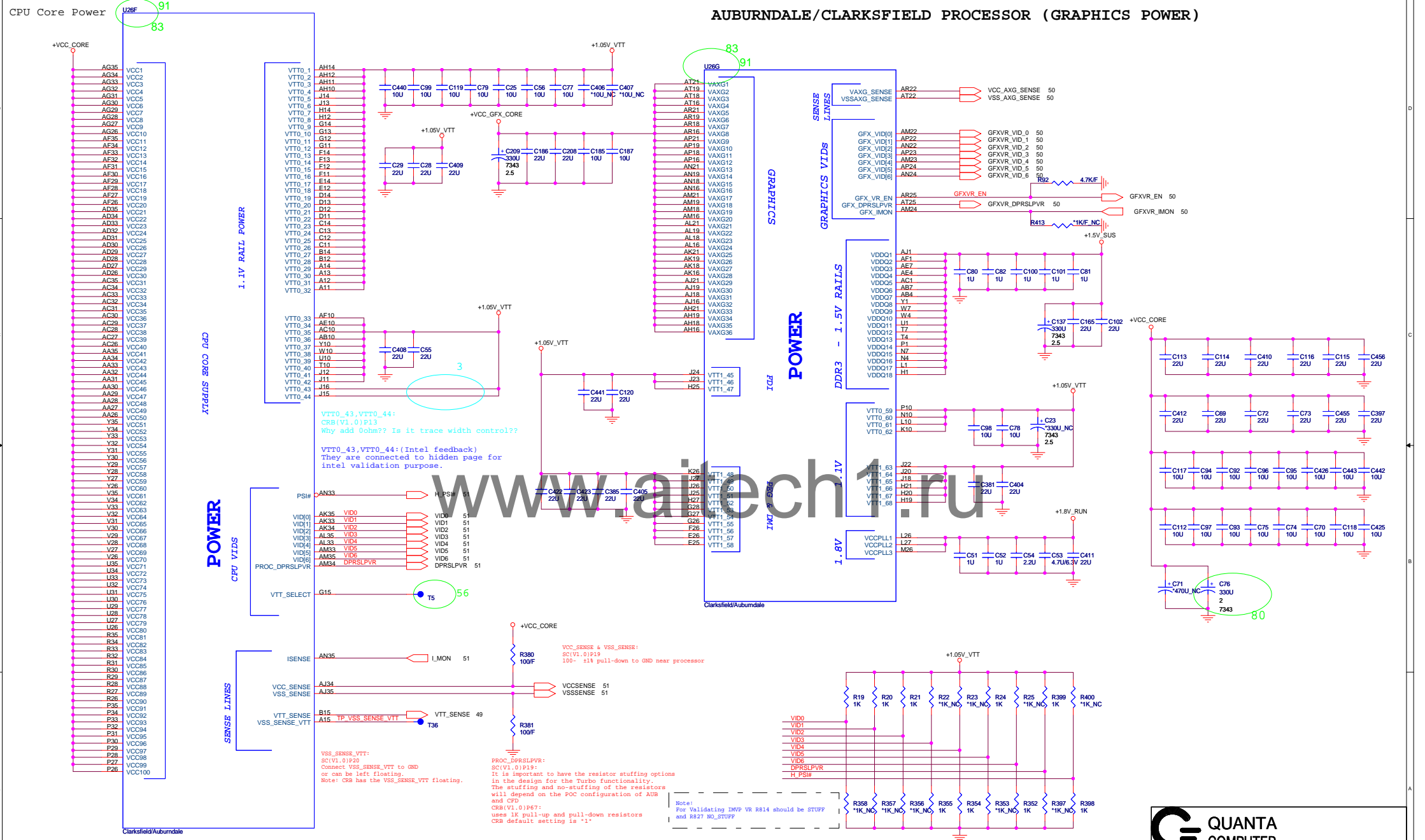
Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

**QUANTA  
COMPUTER**

Title AUBURNDA 2/4		
Size Document Number FM9B	Rev 2B	
Date: Thursday, August 20, 2009	Sheet 4	of 65

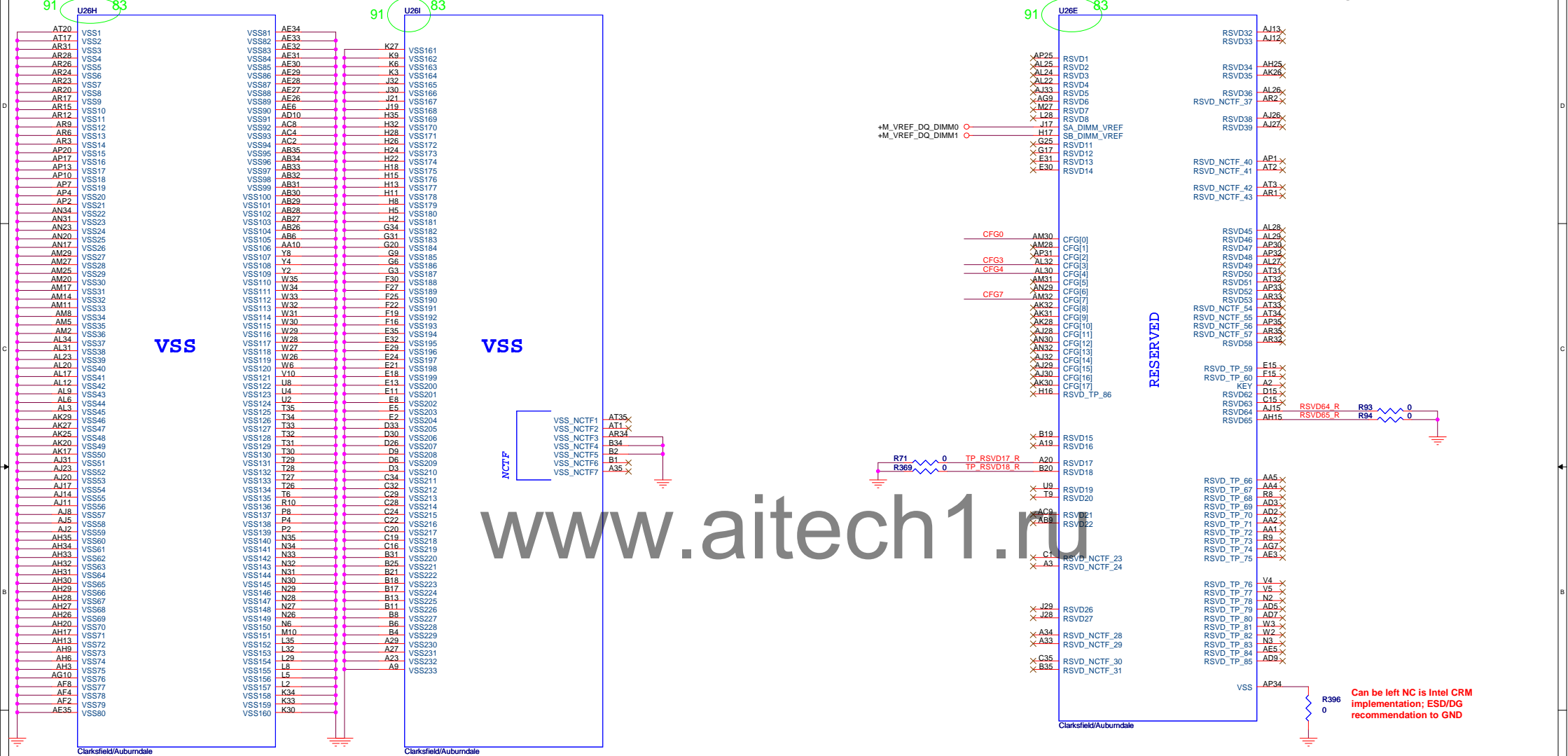
# AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



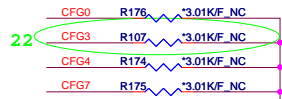
## AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

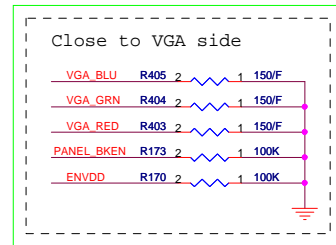
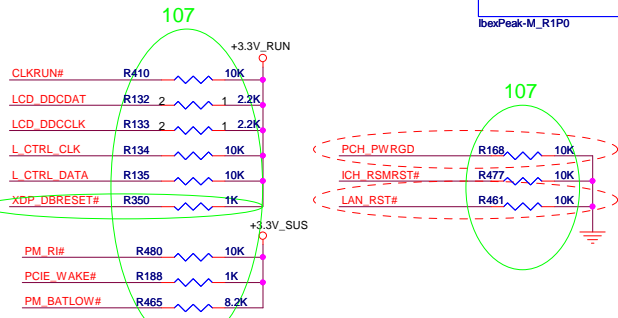
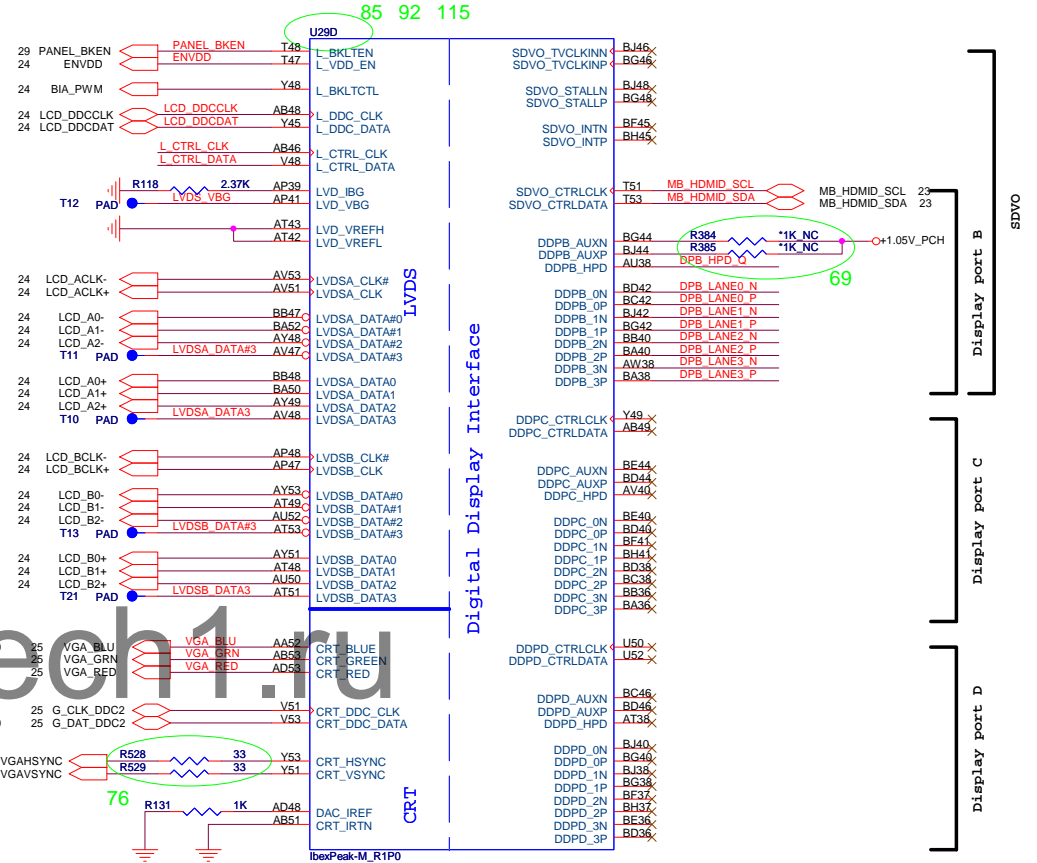


Title AUBURND 4/4		
Size	Document Number FM9B	Rev 2B
Date:	Thursday, August 20, 2009	Sheet 6 of 65

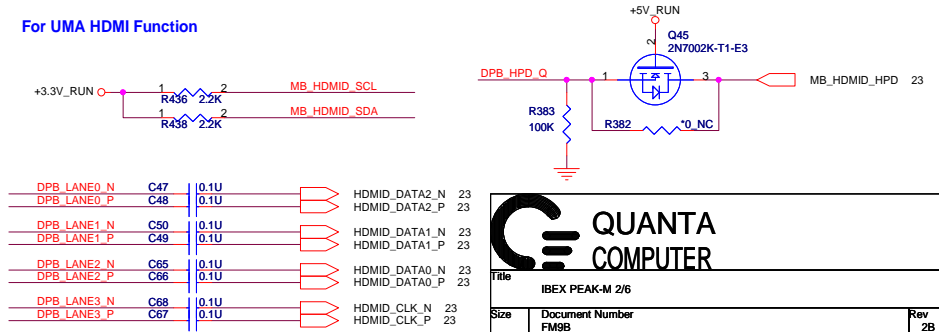
## IBEX PEAK-M (DMI,FDI,GPIO)



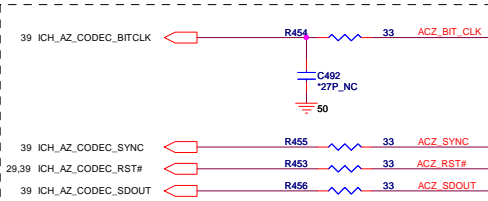
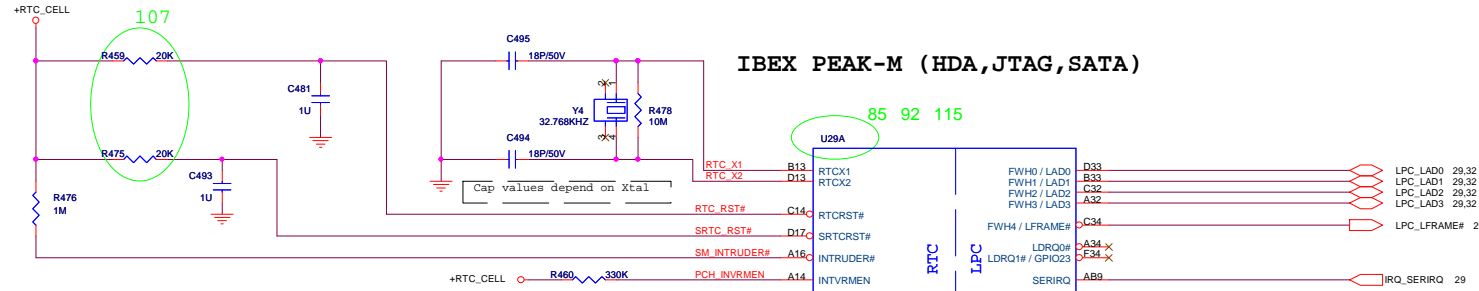
## IBEX PEAK-M (LVDS,DDI)



## For UMA HDMI Function



# IBEX PEAK-M (HDA,JTAG,SATA)

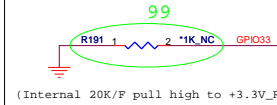


Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

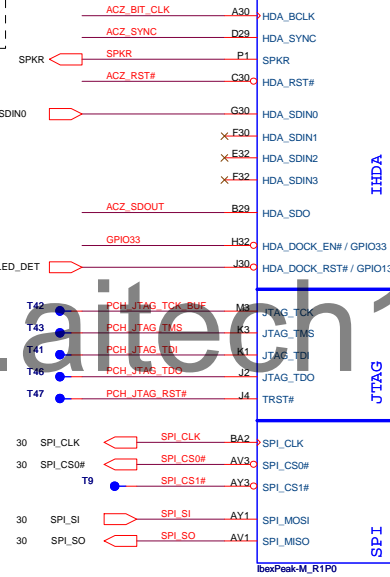
INTVRMEN (Internal Voltage Regulator Enable): This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.

## Flash Descriptor Security Override

GPIO33  
Low = Enabled  
High = Disabled



Note: GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



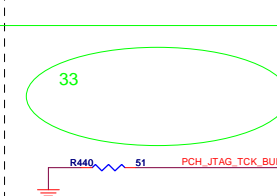
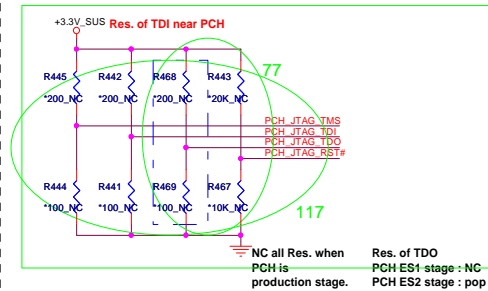
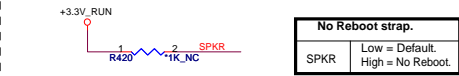
SATA port 2/3 are not support in HM55 . They are only in PM 55

SATA HDD

SATA ODD

E-SATA

Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.



Note: Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

JTAG Test Pads are need to put on the same side of mother board.



IBEX PEAK-M 1/6

Size Document Number FM98

Date: Tuesday, September 01, 2009

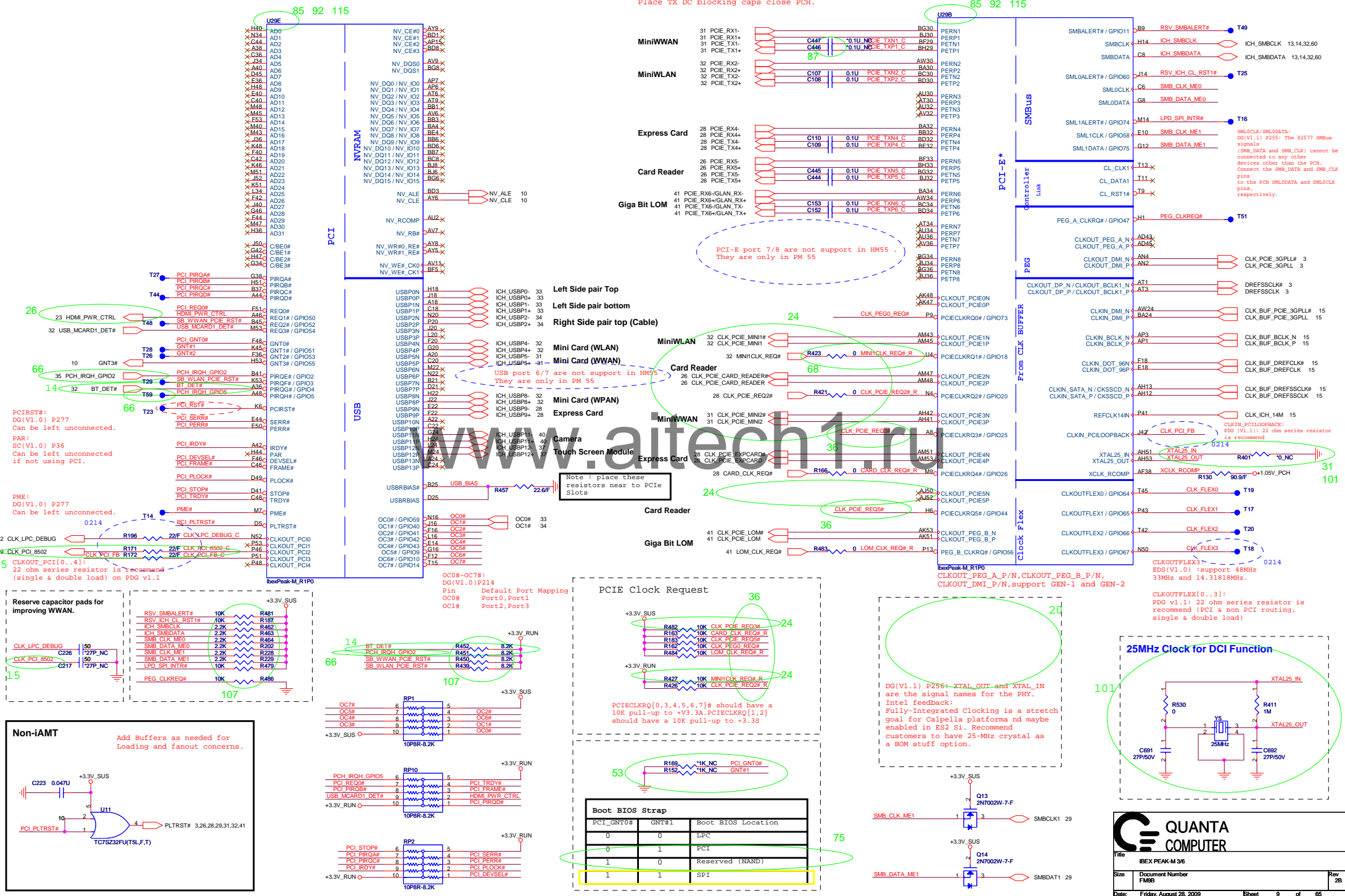
Sheet 8 of 65

Rev 2B

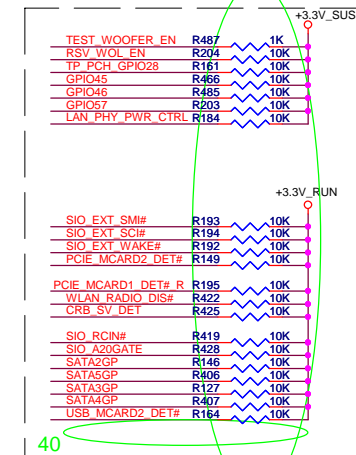
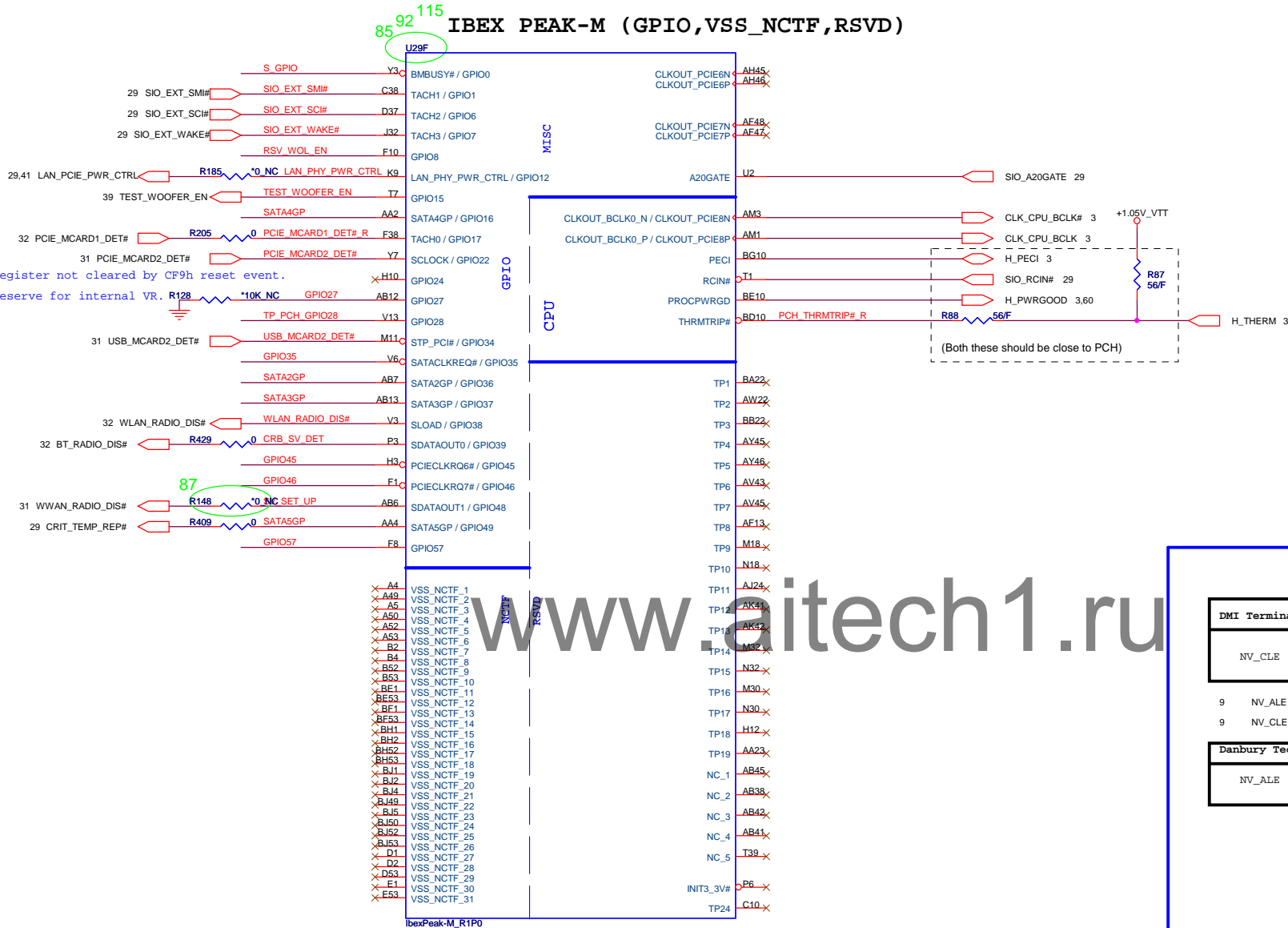
## IBEX PEAK-M (PCI,USB,NVRAM)

## IBEX PEAK-M (PCI-E,SMBUS,CLK)

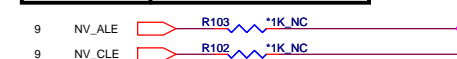
Place TX DC blocking caps close PCH.



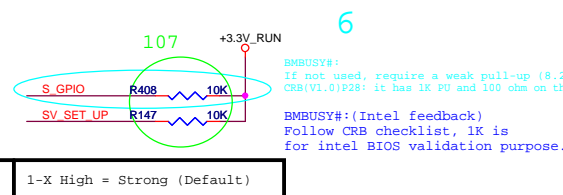
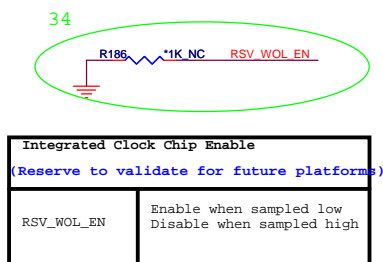
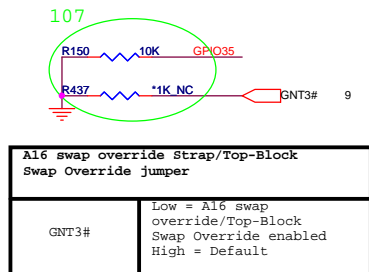
# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

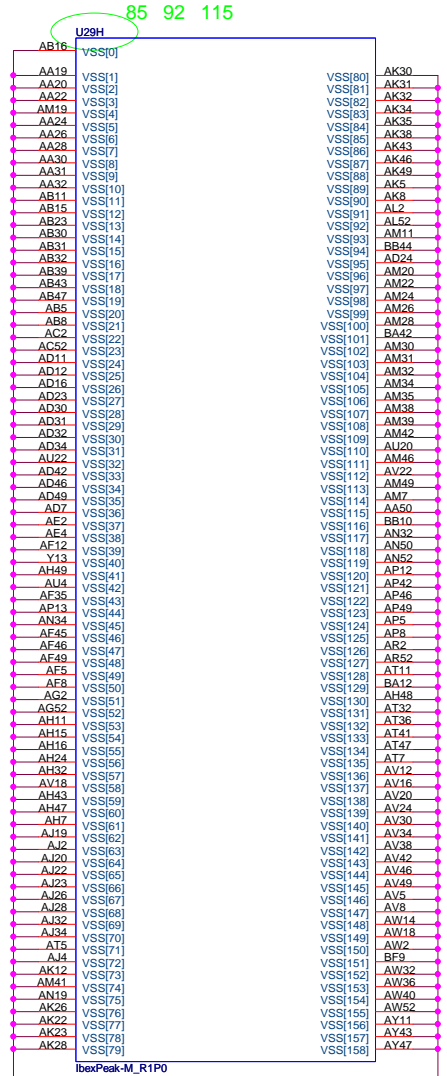


Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

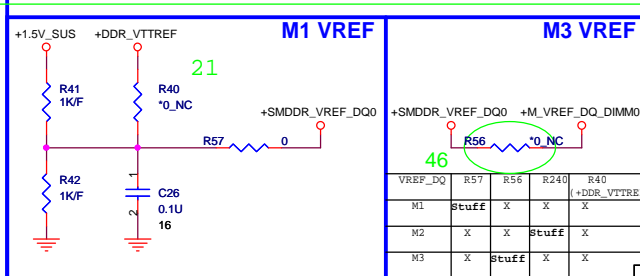
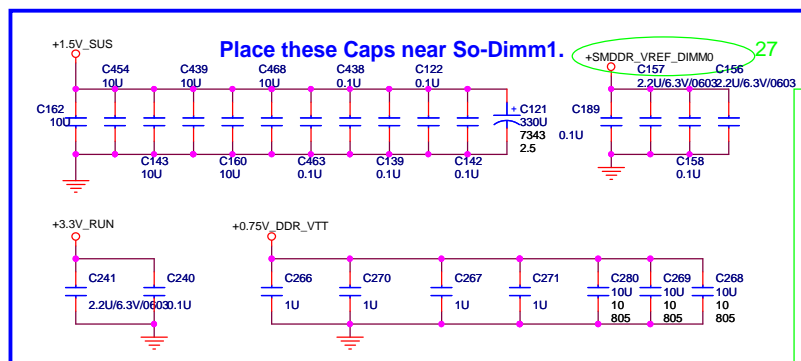
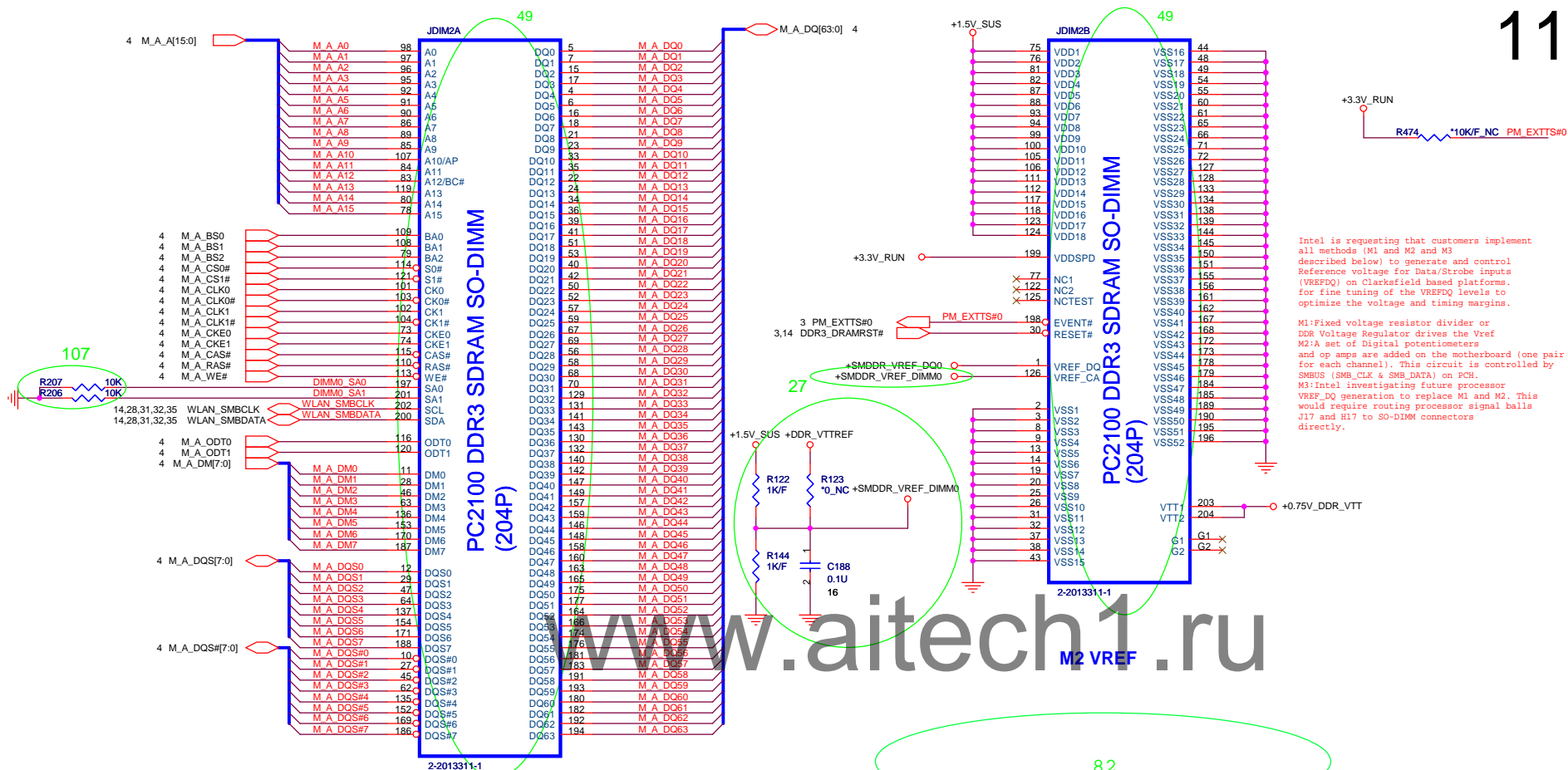




# IBEX PEAK-M (GND)



Title			IBEX PEAK-M 6/6
Size	Document Number	Rev	
	FM9B	2B	
Date:	Friday, August 28, 2009	Sheet	12 of 65

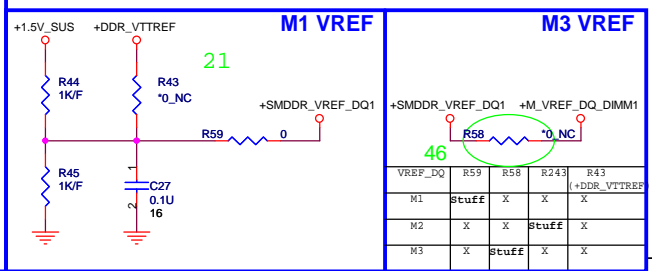
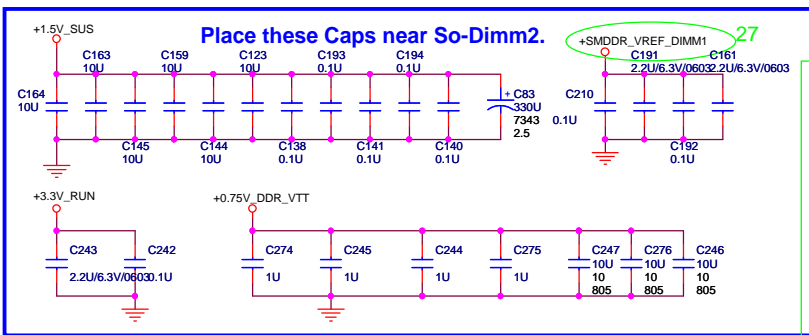
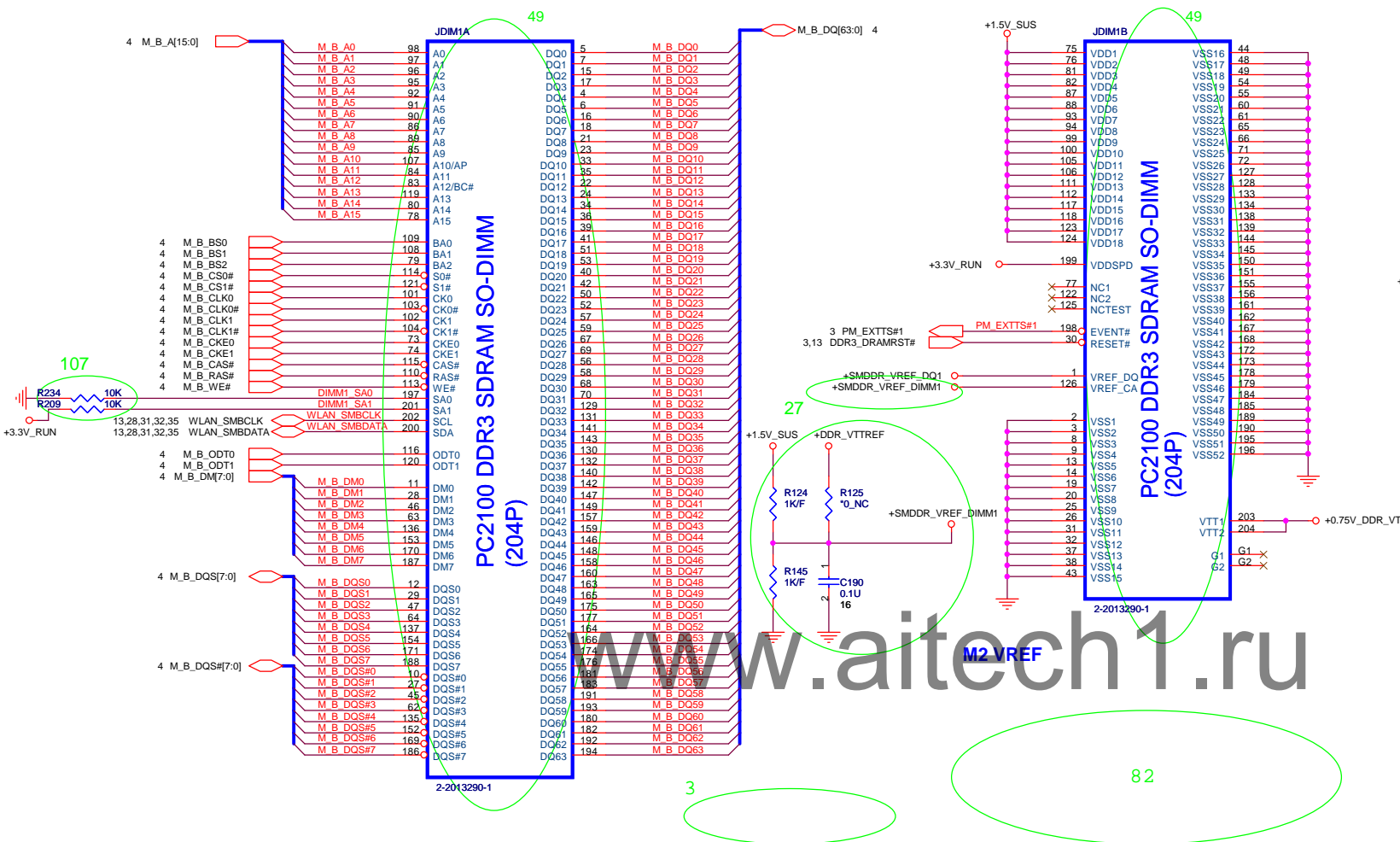


0 +SMDDR\_VREF\_DQ0 +M\_VREF\_DQ\_DIMM0

R56 \*0 NC

46

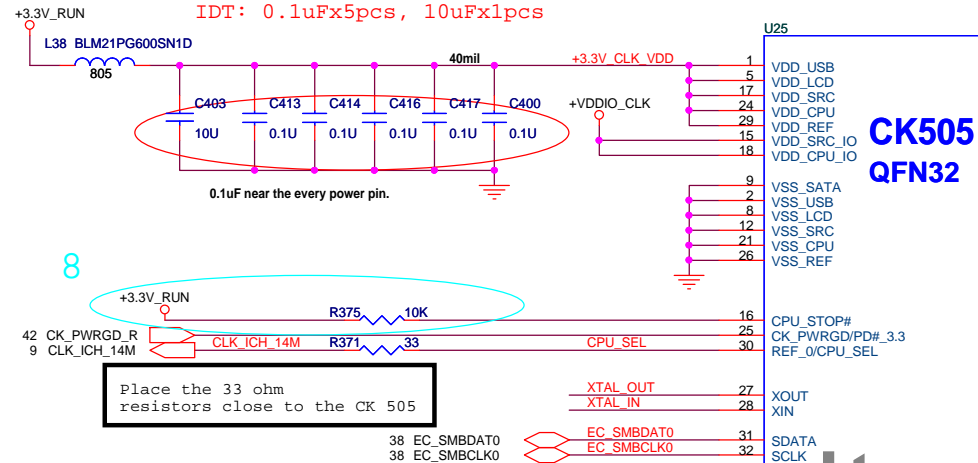
	VREF_DQ	R57	R56	R240	R40
					(+DDR_VTTRE
M1		Stuiff	X	X	X
M2		X	X	Stuiff	X
M3		X	Stuiff	X	X



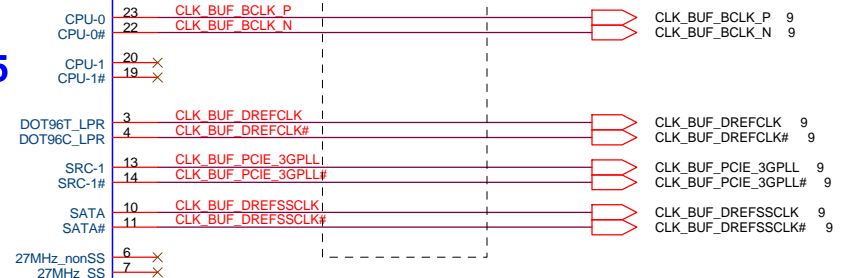
VREF_DQ	R59	R58	R243	R43
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X



Realtek: 0.1uF x 6pcs, 22uF x 1pcs  
IDT: 0.1uF x 5pcs, 10uF x 1pcs



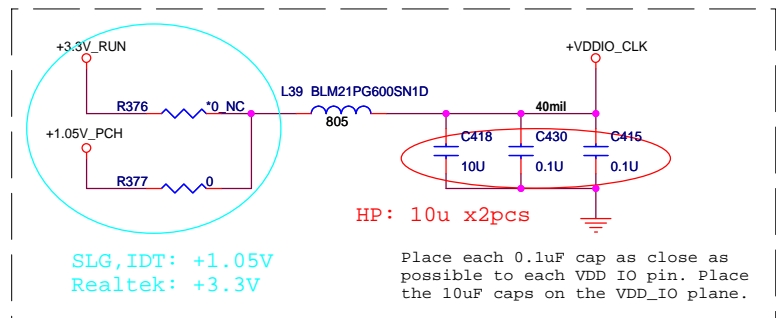
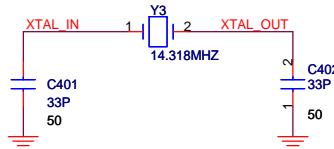
Place within 0.5" of CLKGEN



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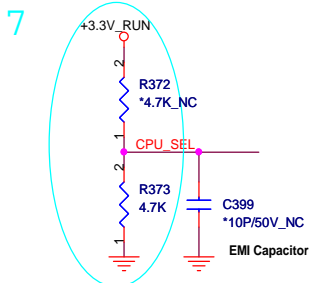
Realtek: 0.1uF x 3pcs, 22uF x 1pcs  
IDT: 0.1uF x 2pcs, 10uF x 1pcs

Add capacitor pads for improving WWAN.



SLG, IDT: +1.05V  
Realtek: +3.3V

+VDDIO\_CLK:  
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.  
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.  
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.




PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU\_SEL:  
SLG date sheet (V0.2) P15:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.  
Realtek date sheet (V1.2) P11:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.  
IDT date sheet (V0.7) P10:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.


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 <b>QUANTA COMPUTER</b>		
Title VGA-M92-XT (PCIe)		
Size	Document Number FM9B	Rev 2B
Date: Thursday, August 20, 2009		
Sheet 16 of 65		

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NUMBER SAME AS DISCRETE

[www.aitech1.ru](http://www.aitech1.ru)


		QUANTA COMPUTER
Title: VGA-MB2-XT (PCIe)		
Size: FM9B	Document Number	Rev: 2B
Date: Thursday, August 20, 2009		Sheet: 17 of 65

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NUMBER SAME AS DISCRETE

[www.aitech1.ru](http://www.aitech1.ru)

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NUMBER SAME AS DISCRETE


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 <b>QUANTA COMPUTER</b>		
Title VGA-M82-XT (PCIe)		
Size	Document Number FM9B	Rev 2B
Date: Thursday, August 20, 2009 1 Sheet 19 of 65		

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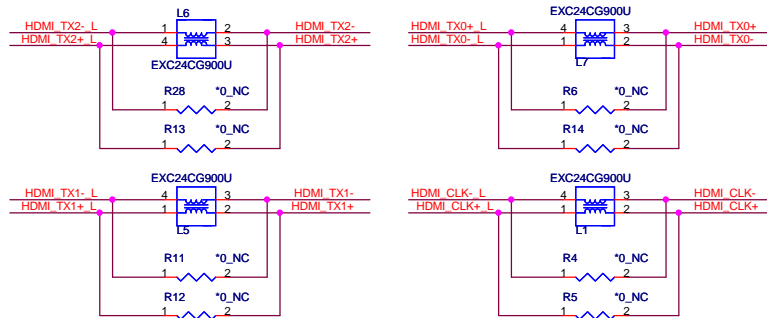
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Title VGA-M92-XT (PCIe)			
Size	Document Number FM9B		Rev 2B
Date Thursday, August 20, 2009		Sheet 21	of 65

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NUMBER SAME AS DISCRETE**  
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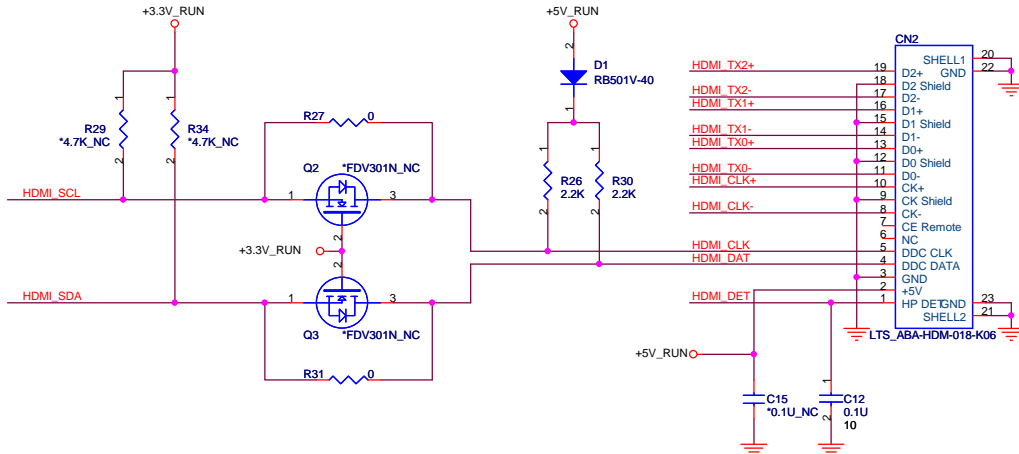
**QUANTA  
COMPUTER**

Title			VGA-M92-XT (PCIe)
Size	Document Number	Rev	
	FM9B	2B	
Date:	Thursday, August 20, 2009	Sheet	22 of 65

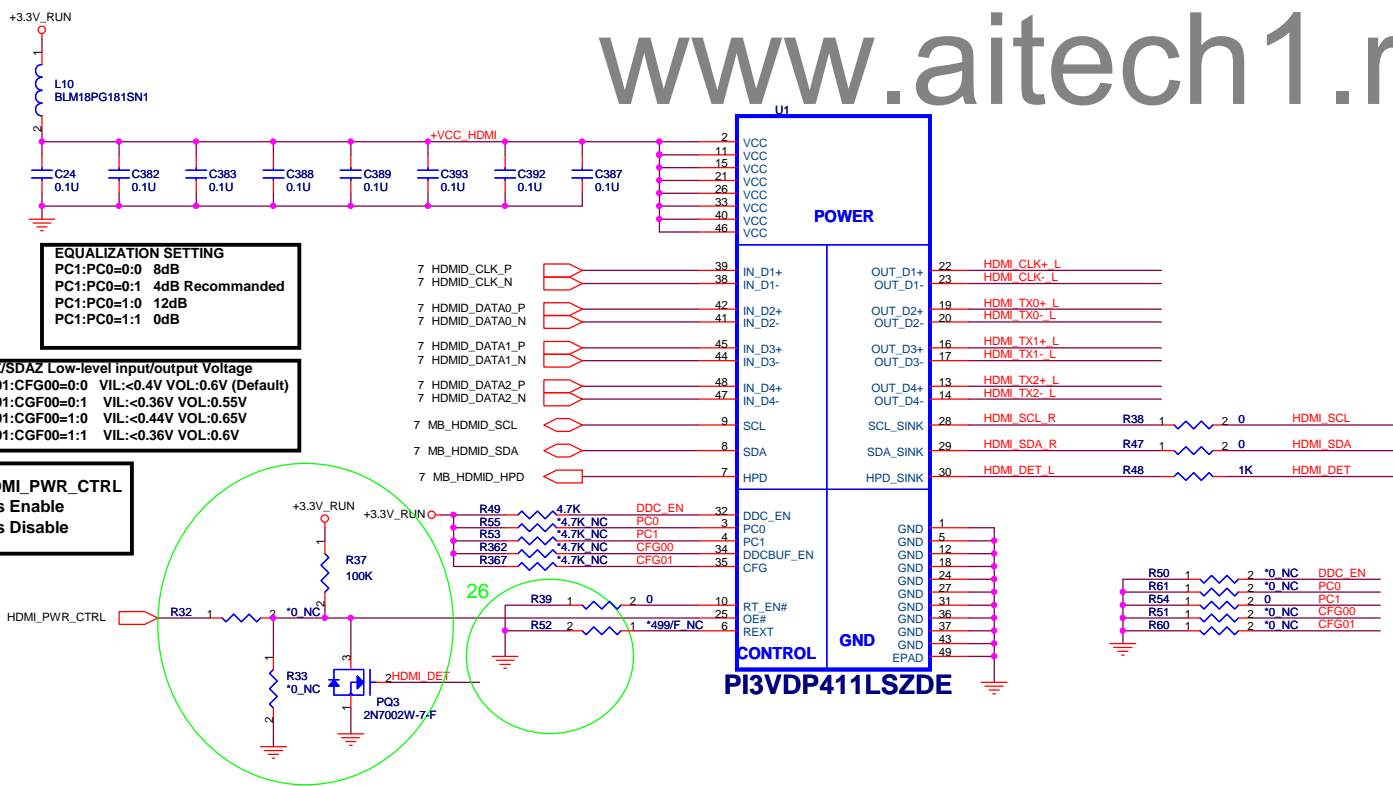


Reserve for EMI and close to HDMI CONN

HDMI_CLK+ L	R7	300	HDMI_CLK C	C16	0.1U	HDMI_CLK- L
HDMI_TX0+ L	R8	300	HDMI_TX0 C	C19	0.1U	HDMI_TX0- L
HDMI_TX1+ L	R15	300	HDMI_TX1 C	C20	0.1U	HDMI_TX1- L
HDMI_TX2+ L	R16	300	HDMI_TX2 C	C22	0.1U	HDMI_TX2- L



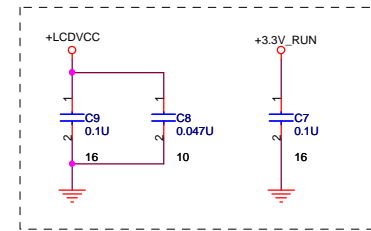
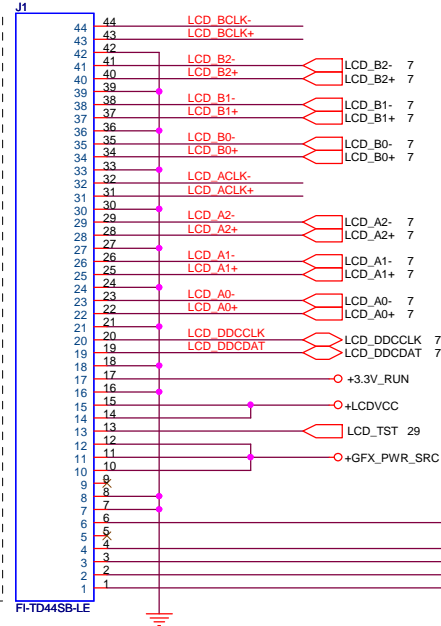
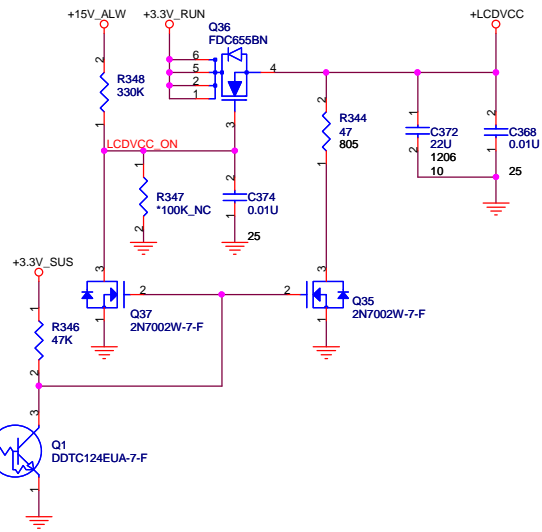
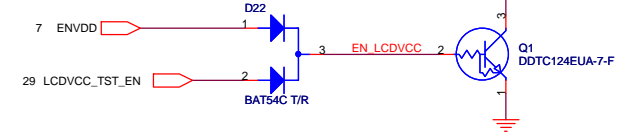
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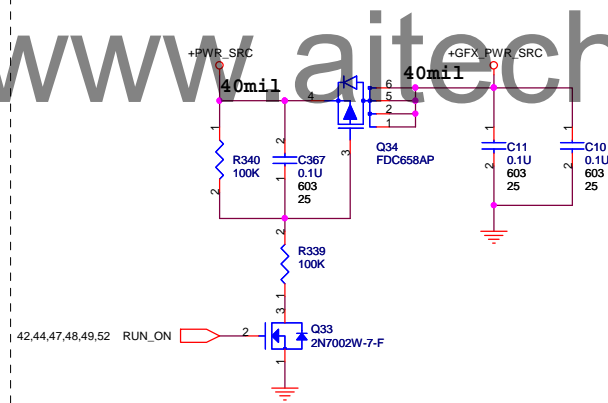
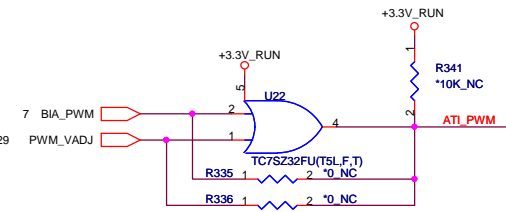
QUANTA  
COMPUTER

File	VGA-M82-S (PCIe)
Size	Document Number FM9B
Date	Thursday, August 20, 2009
Sheet	23 of 65
Rev	2B

Support the new imbedded diagnostics.

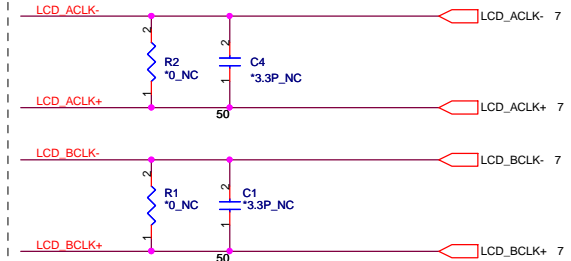


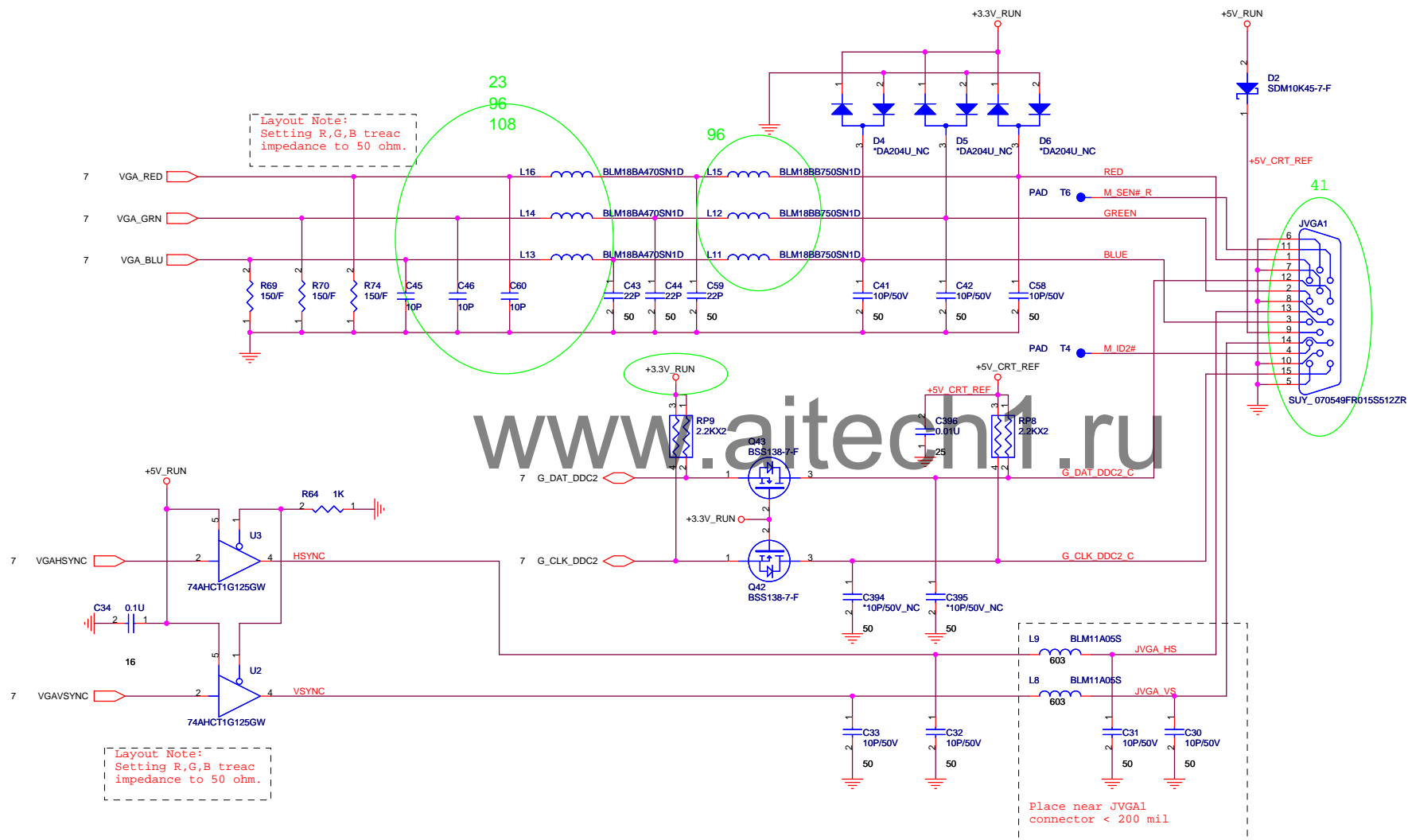
Address : A9H --Contrast  
AAH --Backlight



Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C13	1	2	*3.3P_NC	50	LCD_B0+
LCD_B1-	C3	1	2	*3.3P_NC	50	LCD_B1+
LCD_B2-	C2	1	2	*3.3P_NC	50	LCD_B2+
LCD_A0-	C6	1	2	*3.3P_NC	50	LCD_A0+
LCD_A1-	C5	1	2	*3.3P_NC	50	LCD_A1+
LCD_A2-	C14	1	2	*3.3P_NC	50	LCD_A2+






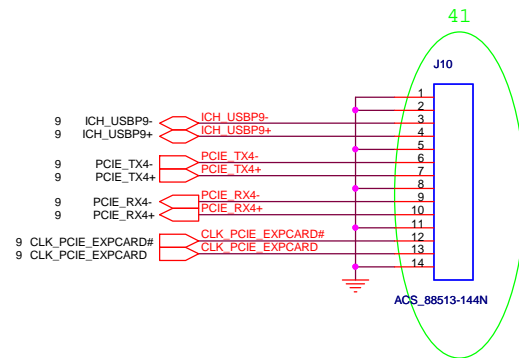
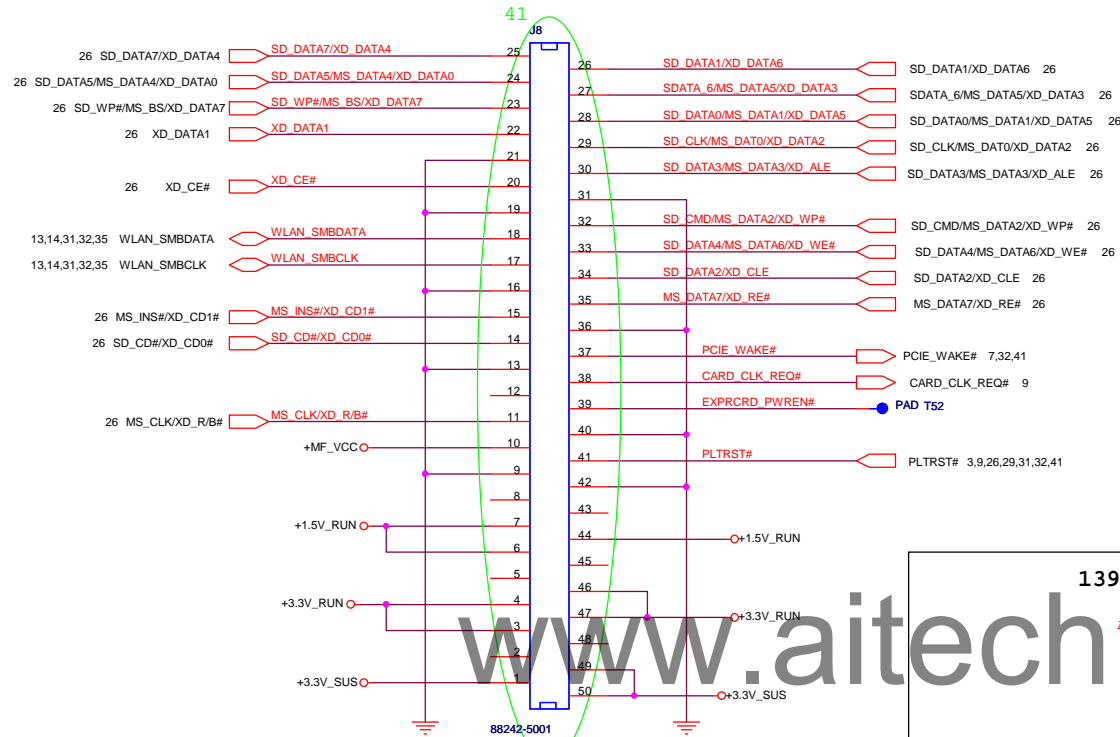


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NUMBER SAME AS DISCRETE**

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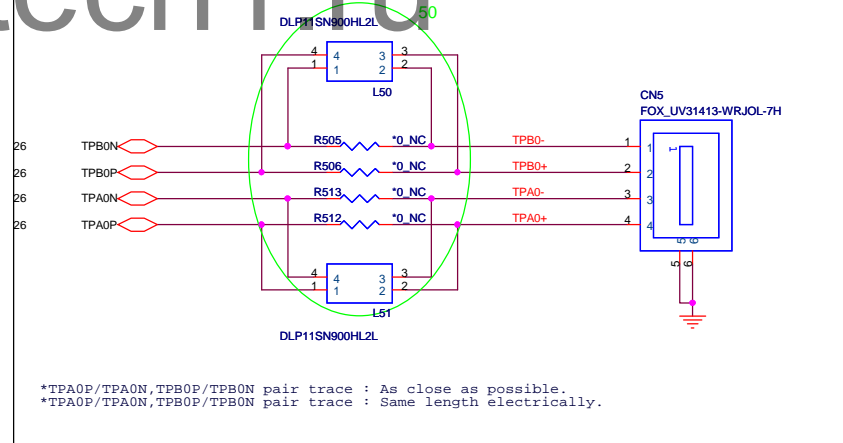
			<b>QUANTA COMPUTER</b>		
Title IEEE 1394					
Size	Document Number FM9B				Rev 2B
Date: Thursday, August 20, 2009			Sheet 27 of 65		

# Express Card/CARD READER



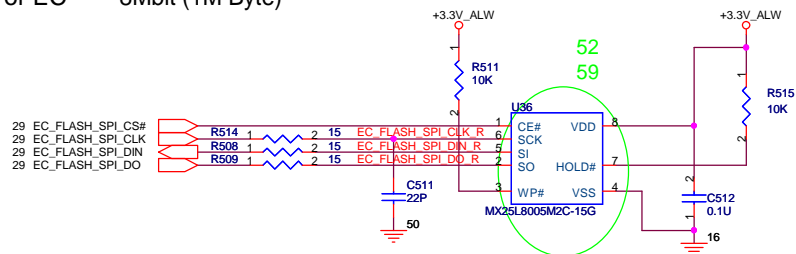
## 1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

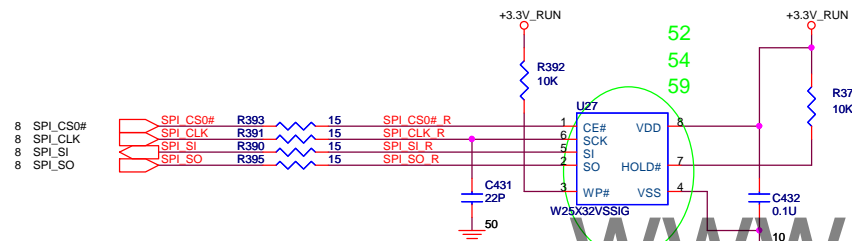




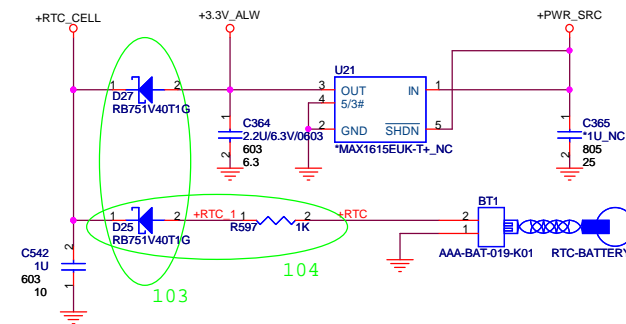
# For EC 8Mbit (1M Byte)



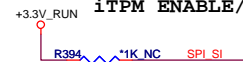
# For PCH 32Mbit (4M Byte)



# RTC BATTERY



# iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



Ultra I/O Controller ECE5028

Size Document Number FM9B

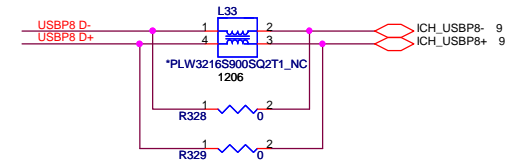
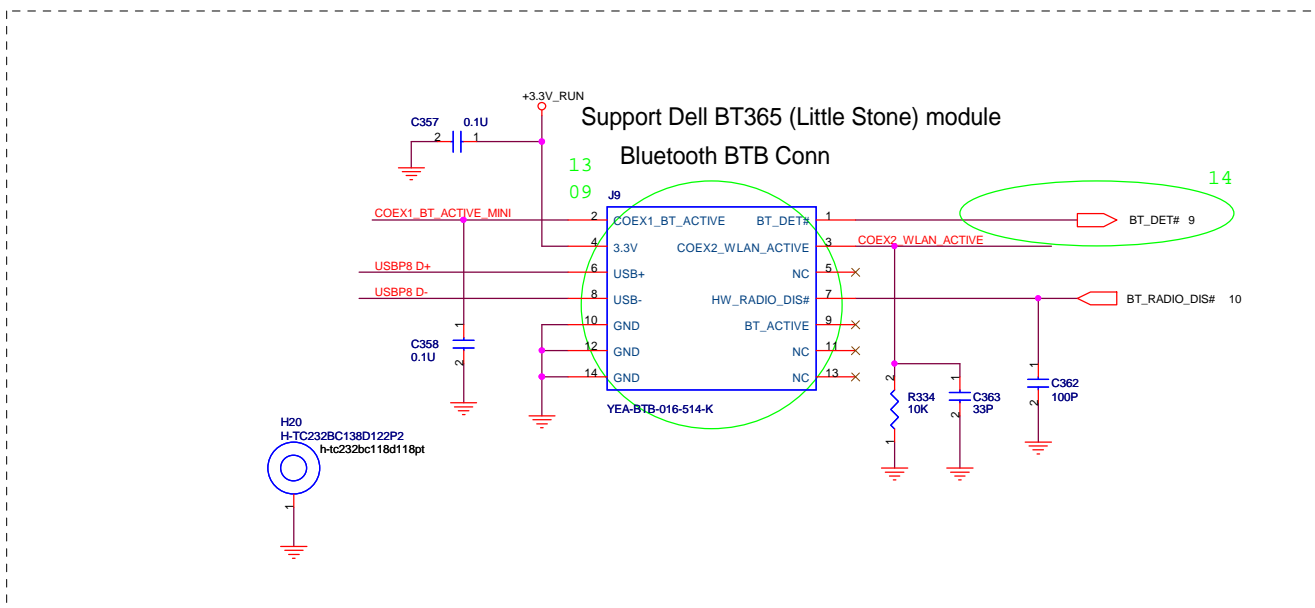
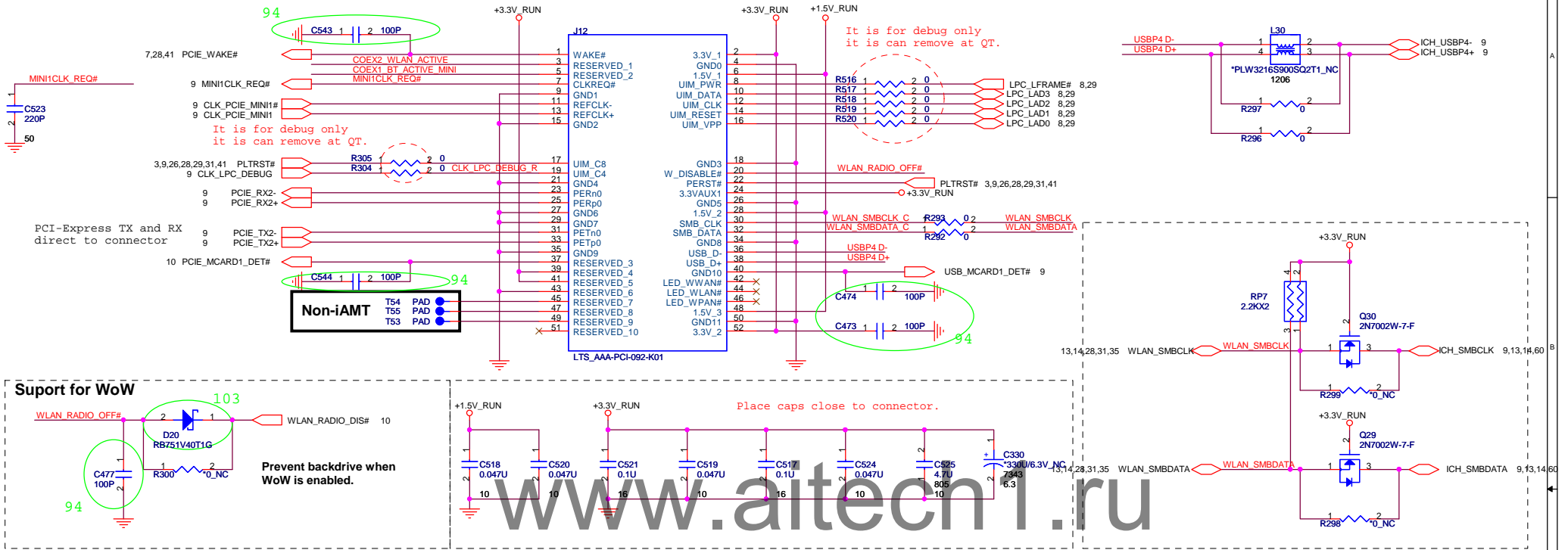
Date: Friday, September 04, 2009

Sheet 30 of 65

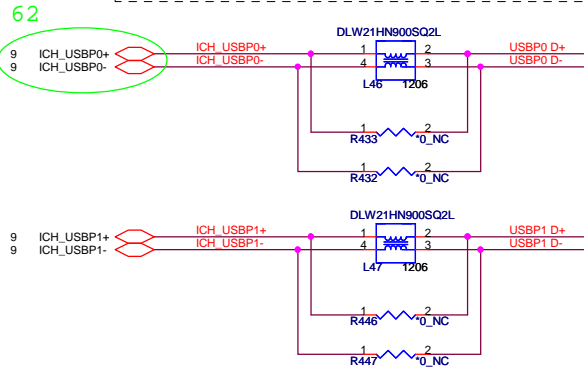
Rev 2B



# MiniCard WLAN connector

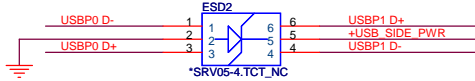


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



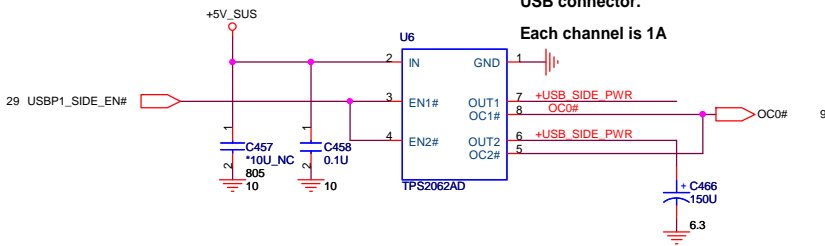
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



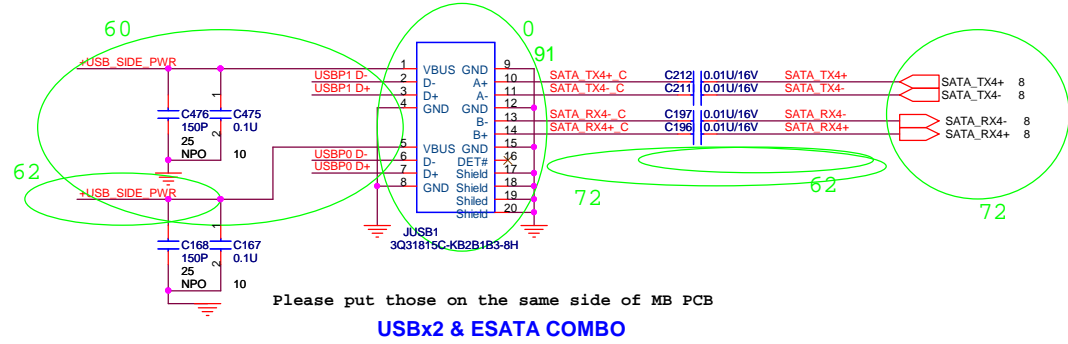
Place one 150uF cap by each USB connector.

Each channel is 1A



Side External USBX2

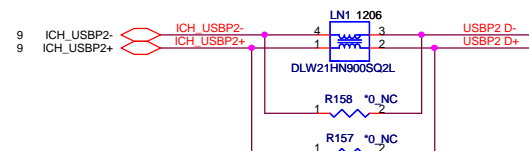
PN is old, Because New Part can't ready before SST build.



USB BUS SW

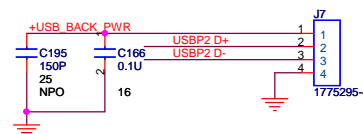
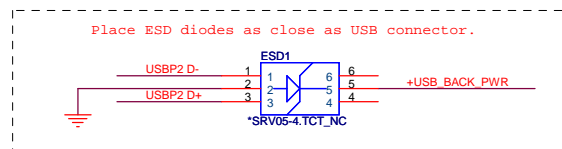
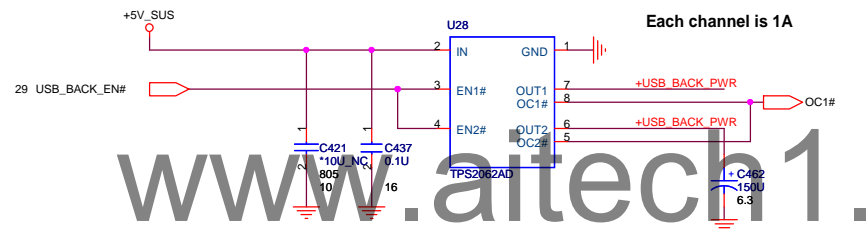
E-SATA Re-driver





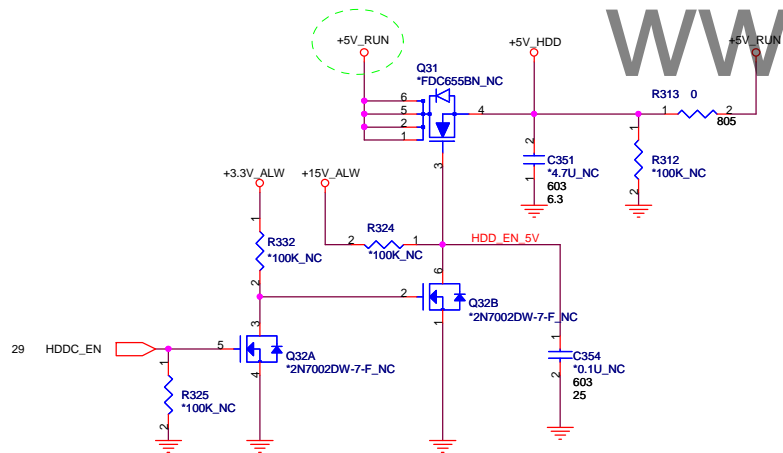
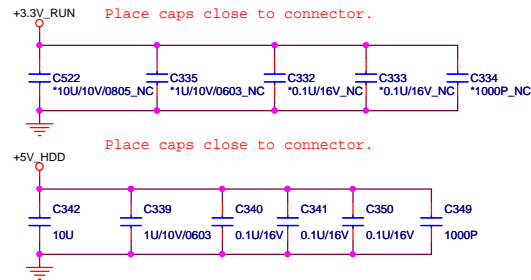
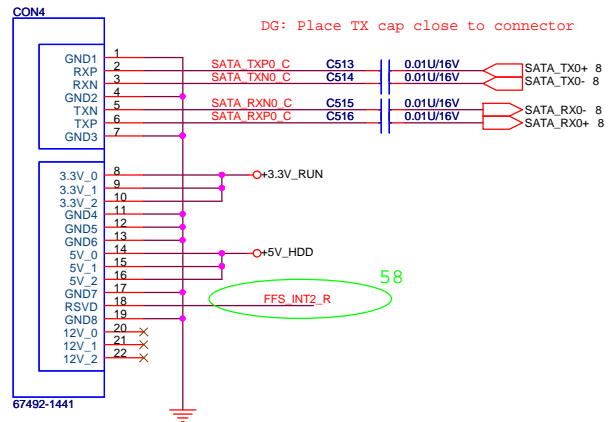
Place one 150uF cap by each  
USB connector.

Each channel is 1A

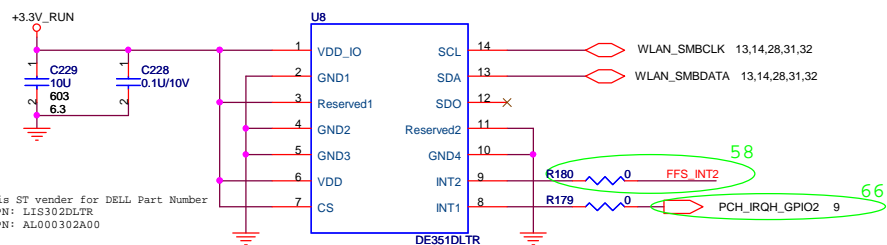


Title		
Right USB		
Size	Document Number	Rev
	FM9B	2B
Date:	Thursday, August 20, 2009	Sheet 34 of 65

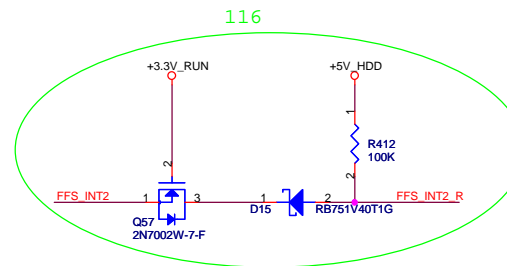
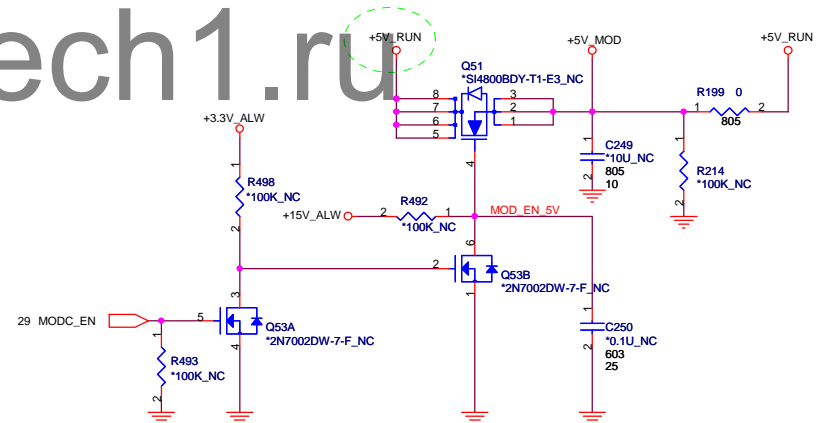
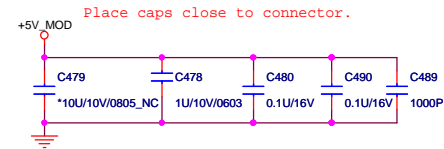
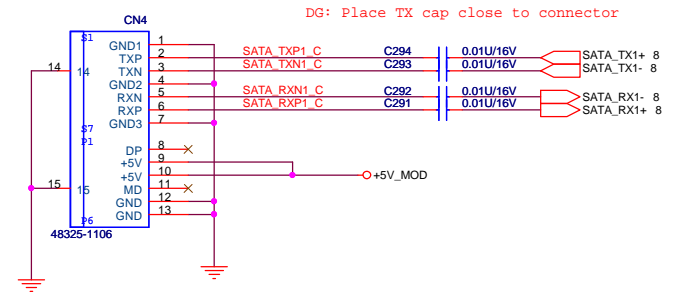
## SATA Connector.



## 3-axis Fall Sensor (HDD data protector)

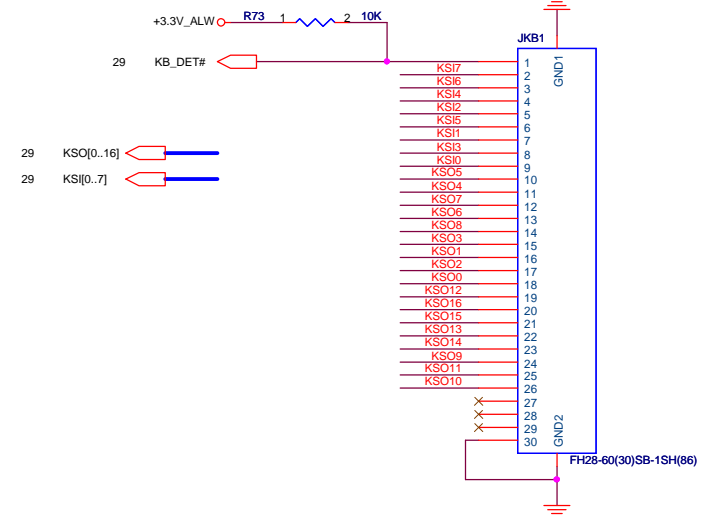


## ODD Connector

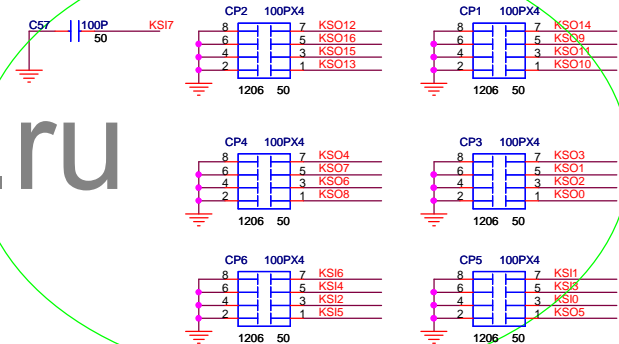


Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FM9B	2B	
Date:	Tuesday, September 01, 2009	Sheet	35 of 65

# KEYBOARD CONNECTOR



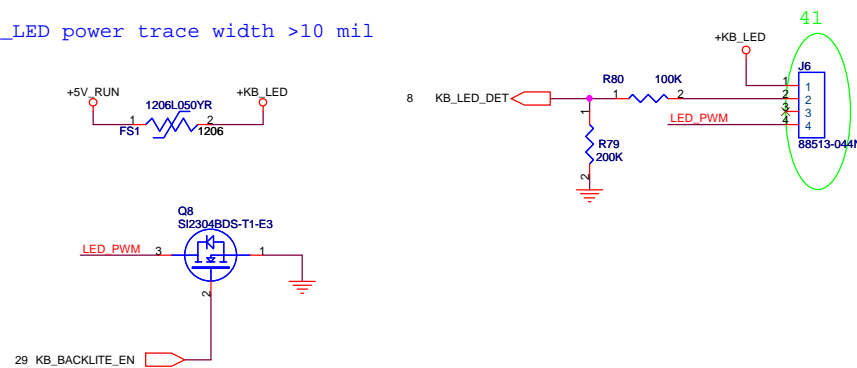
63



100P CAPS CLOSE TO JKB1

## Key board illumination

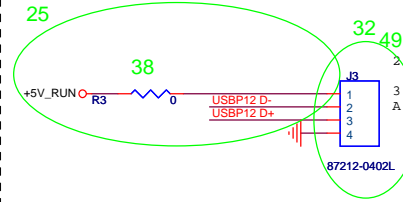
+KB\_LED power trace width >10 mil



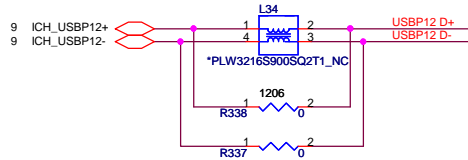
Title TOUCH PAD, BULE TOOTH & FIR		
Size	Document Number FM9B	Rev 2B
Date: Thursday, August 20, 2009	Sheet 36	of 65

## Touch Screen Module

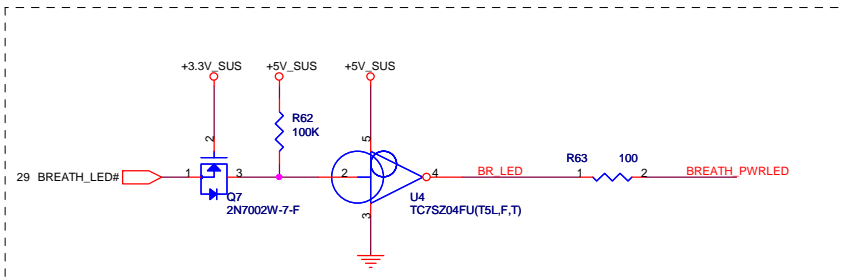
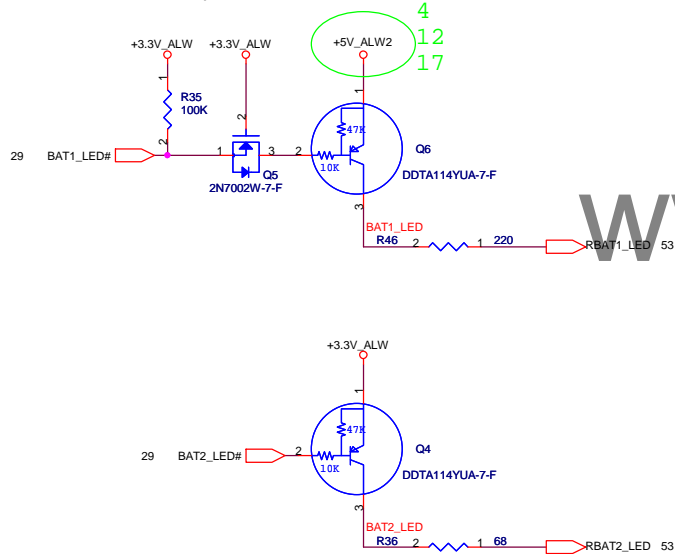
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
  2. Maximum cable resistance on VCC, GND should be 150m ohm.
  3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



Need check the connector footprint and symbol.



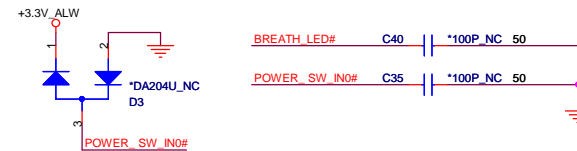
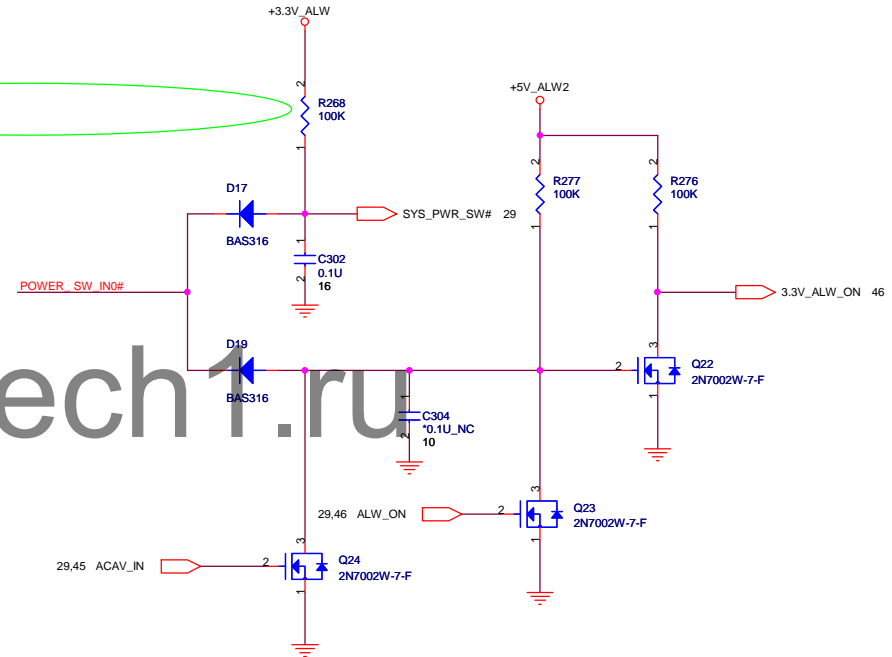
### Battery status.

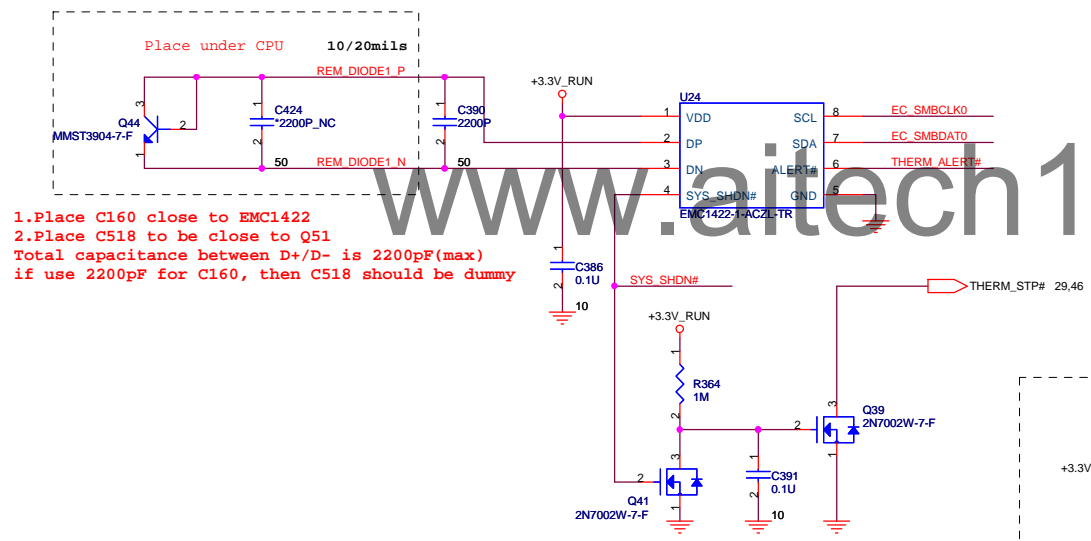
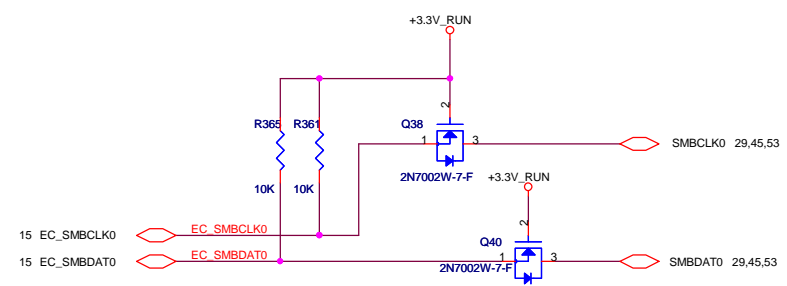
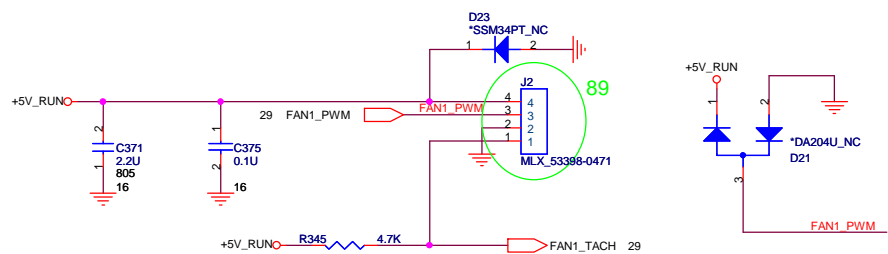


### Power button Cable

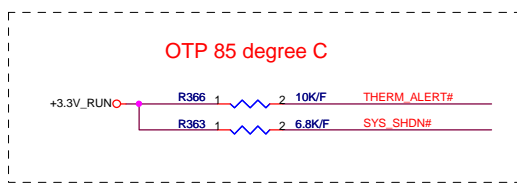


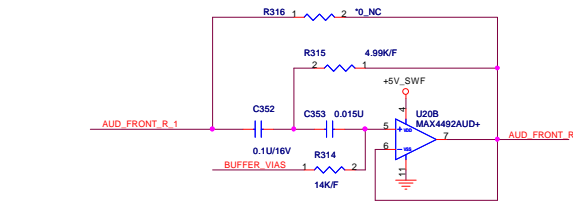
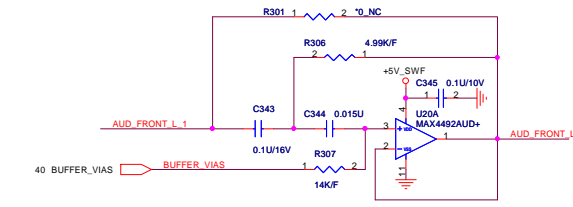
### 3VALW ON POWER LOGIC



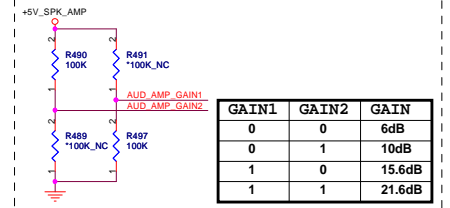
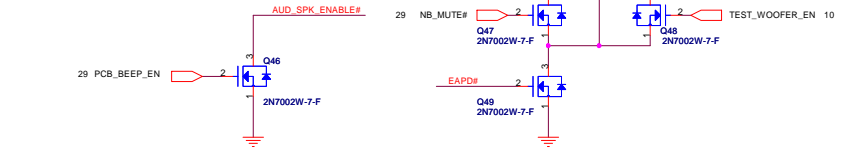


1.Place C160 close to EMC1422  
2.Place C518 to be close to Q51  
Total capacitance between D+/D- is 2200pF(max)  
if use 2200pF for C160, then C518 should be dummy

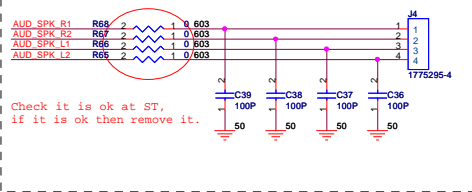
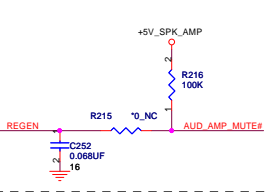
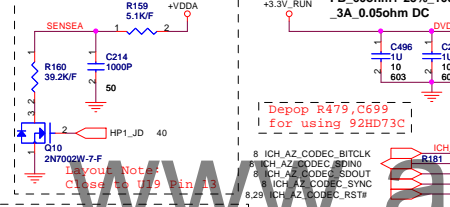
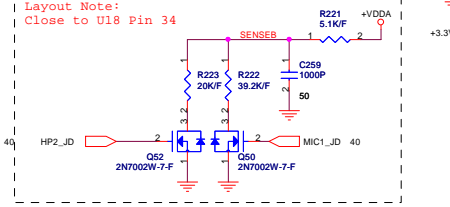
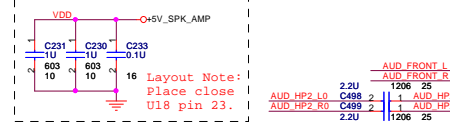




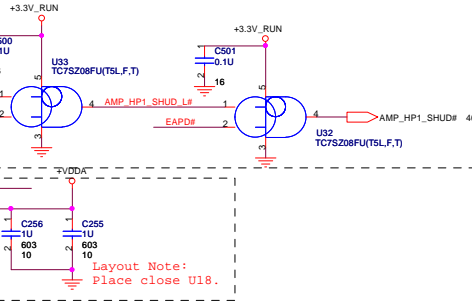
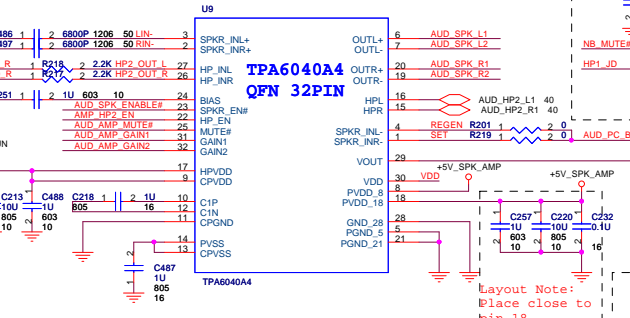
EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H



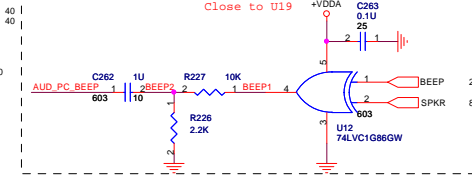
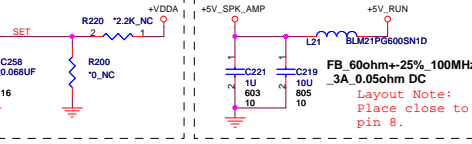
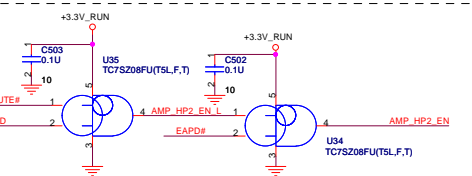
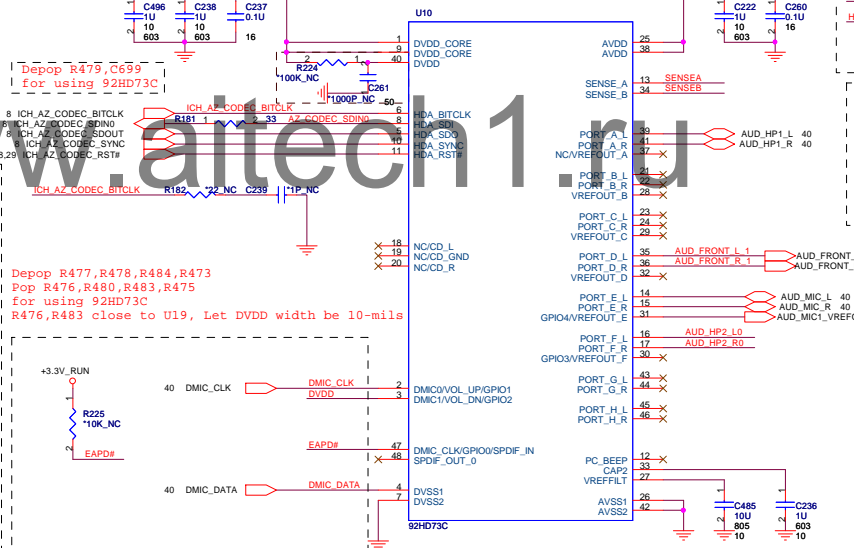
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



### INTERNAL SPEAKER AMP

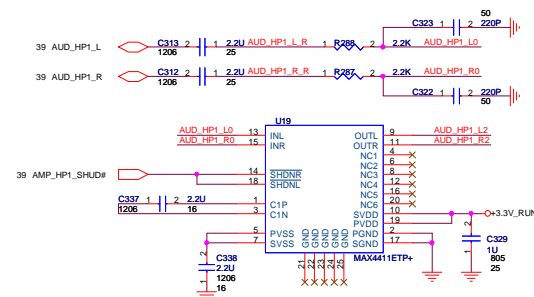
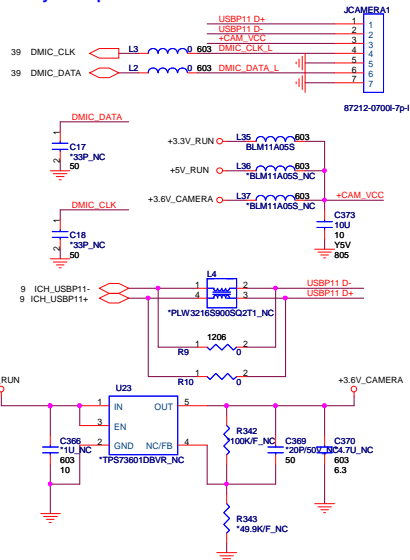


### AZALIA (HD) CODEC

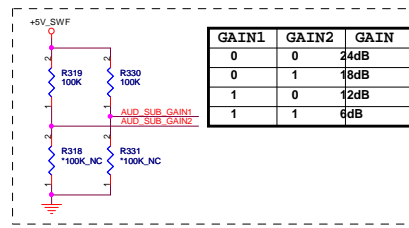


File	Azalia CODEC	Rev	2B
Size	Document Number FM98	Date	Thursday, August 20, 2009
		Sheet	39 of 66


## Array Microphone & Camera



## INTERNAL SUBWOOFER AMP

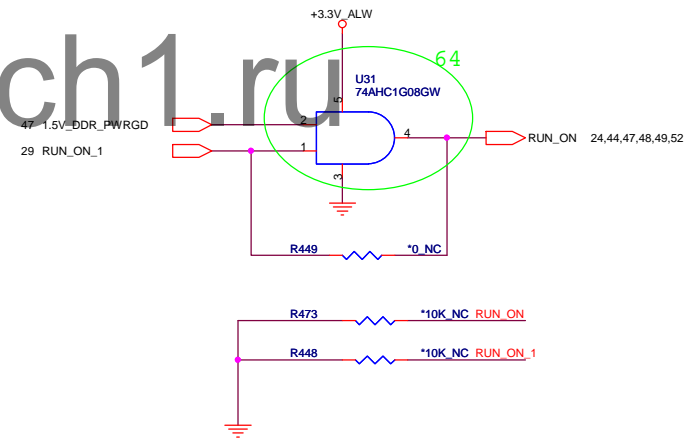
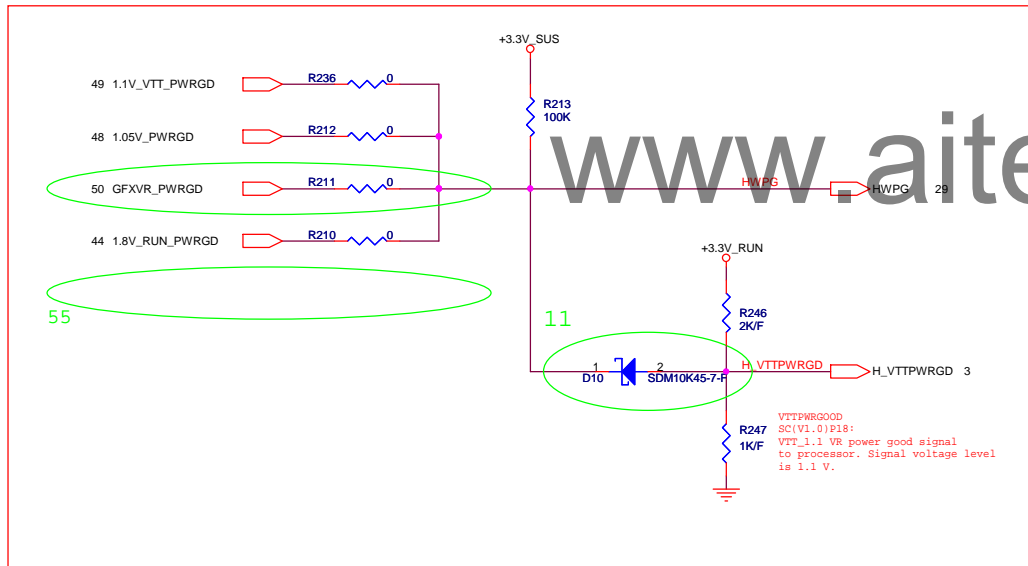
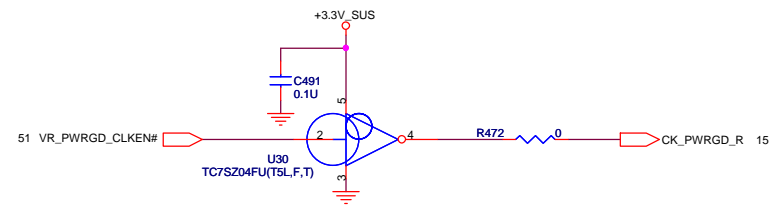
[illegible]

73




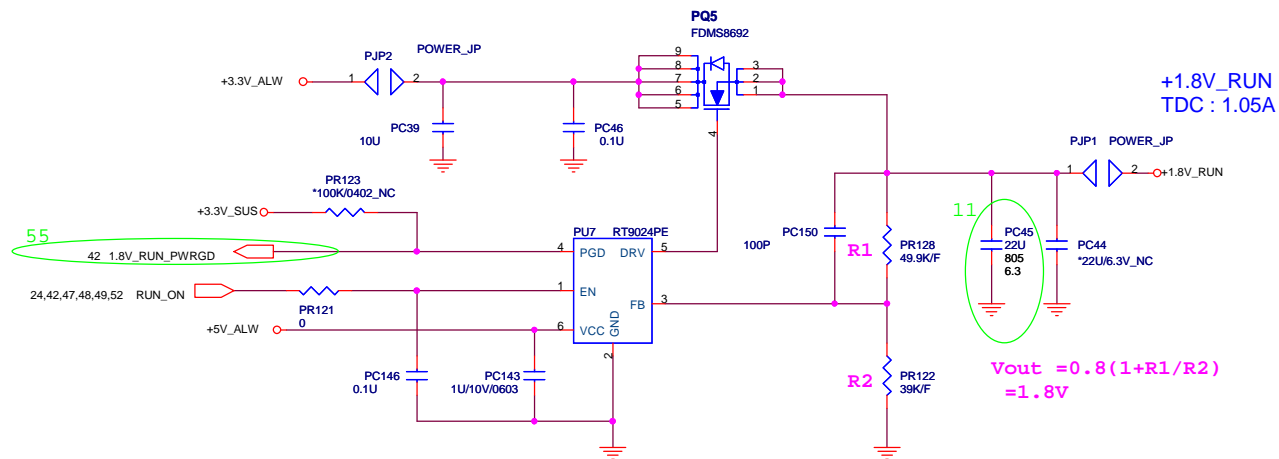
The diagram shows a circuit connection between two power pins: +5V\_SWF and +5V\_SPK\_AMP. A resistor labeled R126 with a value of 603 is connected between these two pins. The connection is highlighted with a green oval and the number 73.





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 QUANTA COMPUTER		
Title Battery Selector		
Size	Document Number FM9B	Rev 2B
Date:	Thursday, August 20, 2009	Sheet 43 of 65

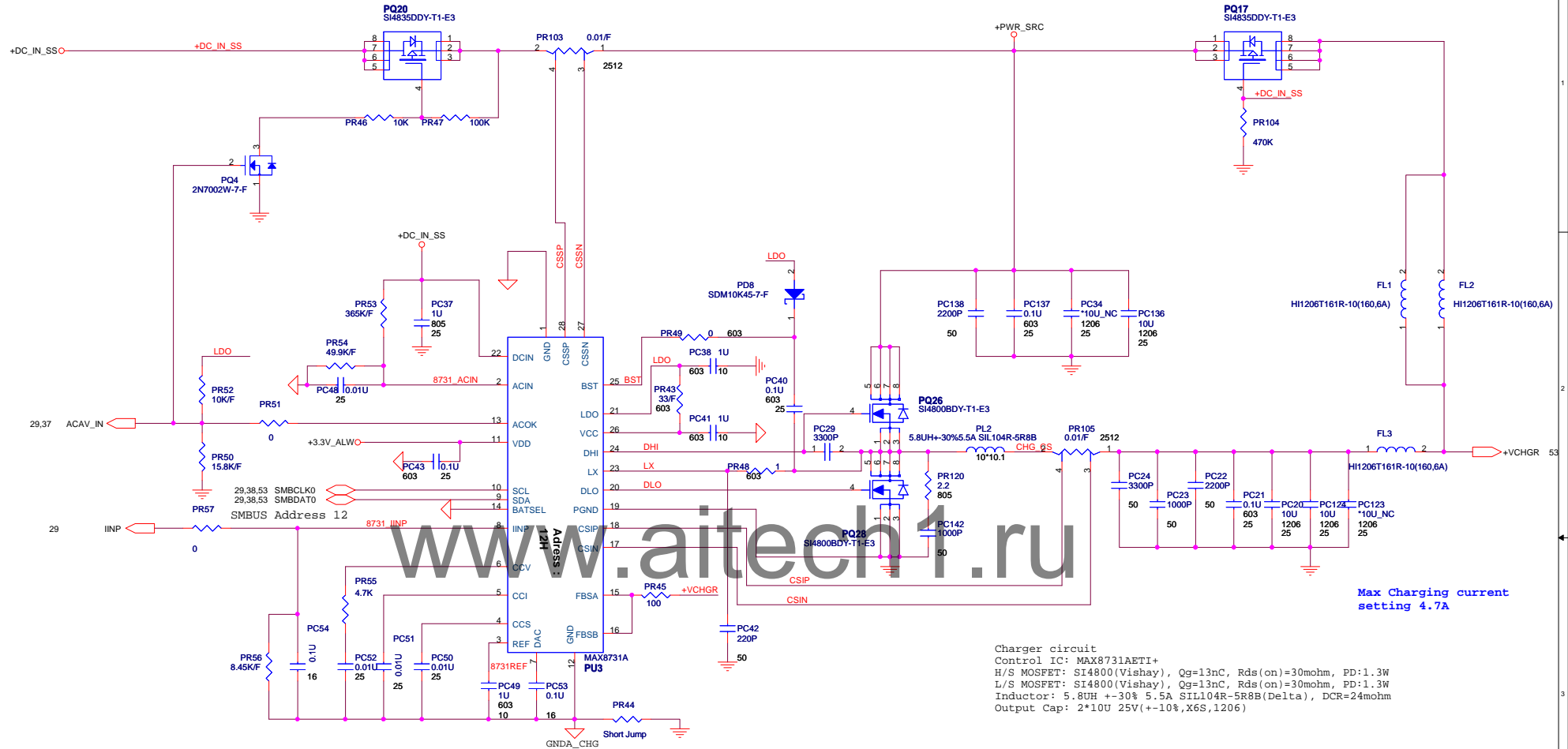


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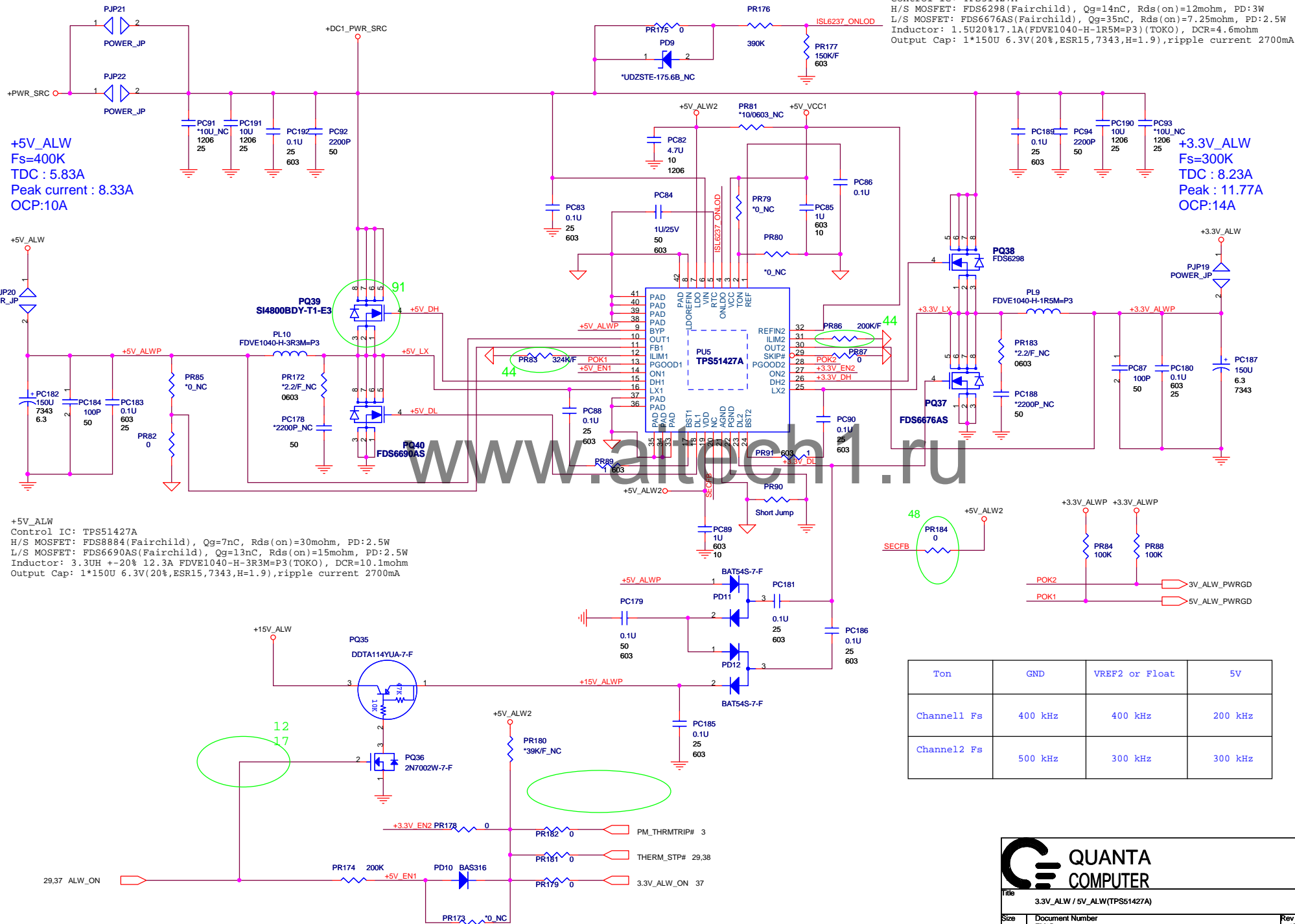
Title		
+1.8V_RUN(RT9024)		
Size	Document Number	Rev
FM9B		2B
Date:	Thursday, August 20, 2009	Sheet 44 of 65

Continuous current : 13A  
Rds(on) : 18mohm

Continuous current : 13A  
Rds(on) : 18mohm



Title			
Charger (MAX8731)			
Size	Document Number	Rev	
FM9B		2B	
Date:	Thursday, August 20, 2009	Sheet	45 of 65



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz



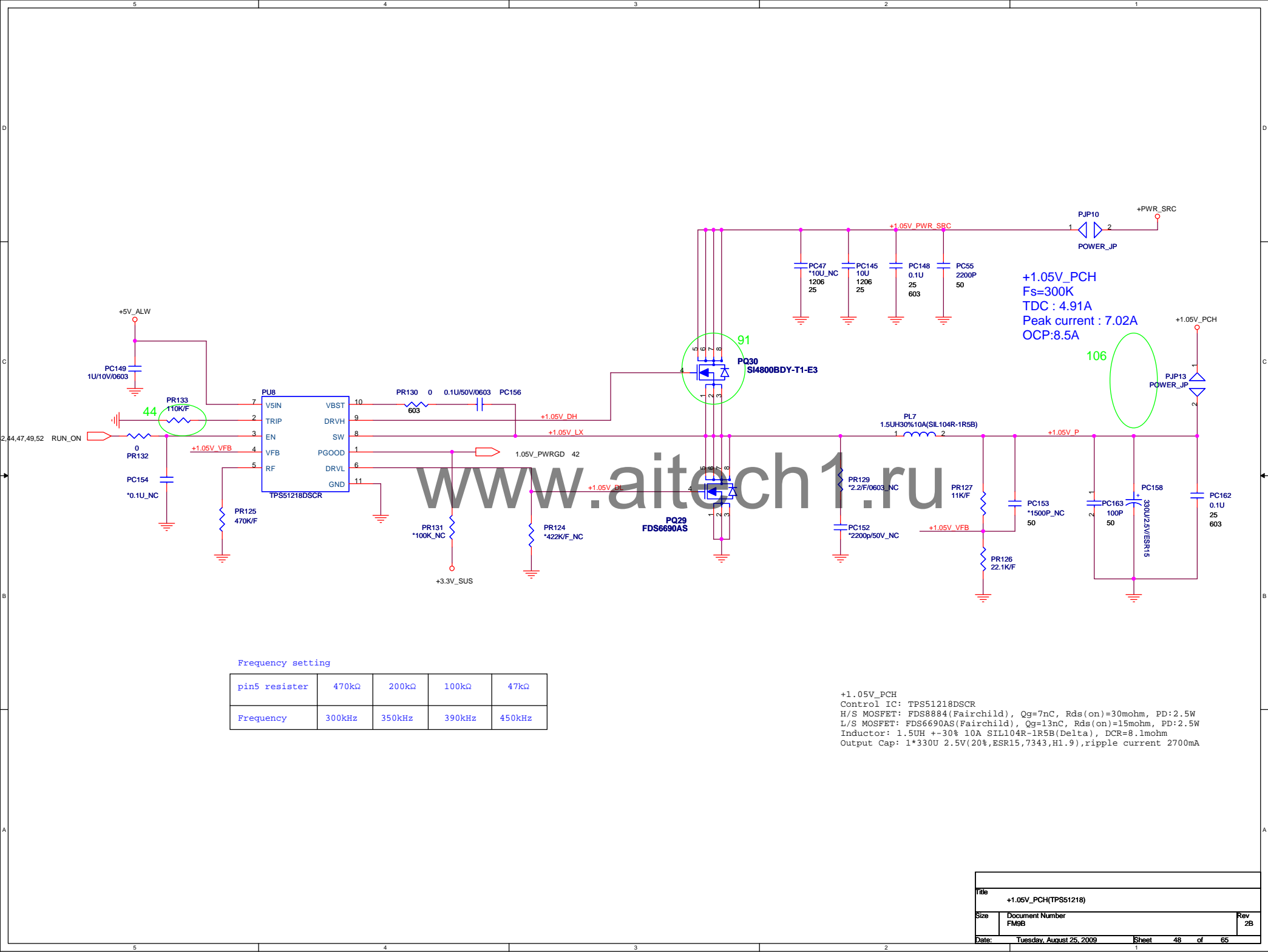
Title  
3.3V\_ALW / 5V\_ALW(TPS51427A)

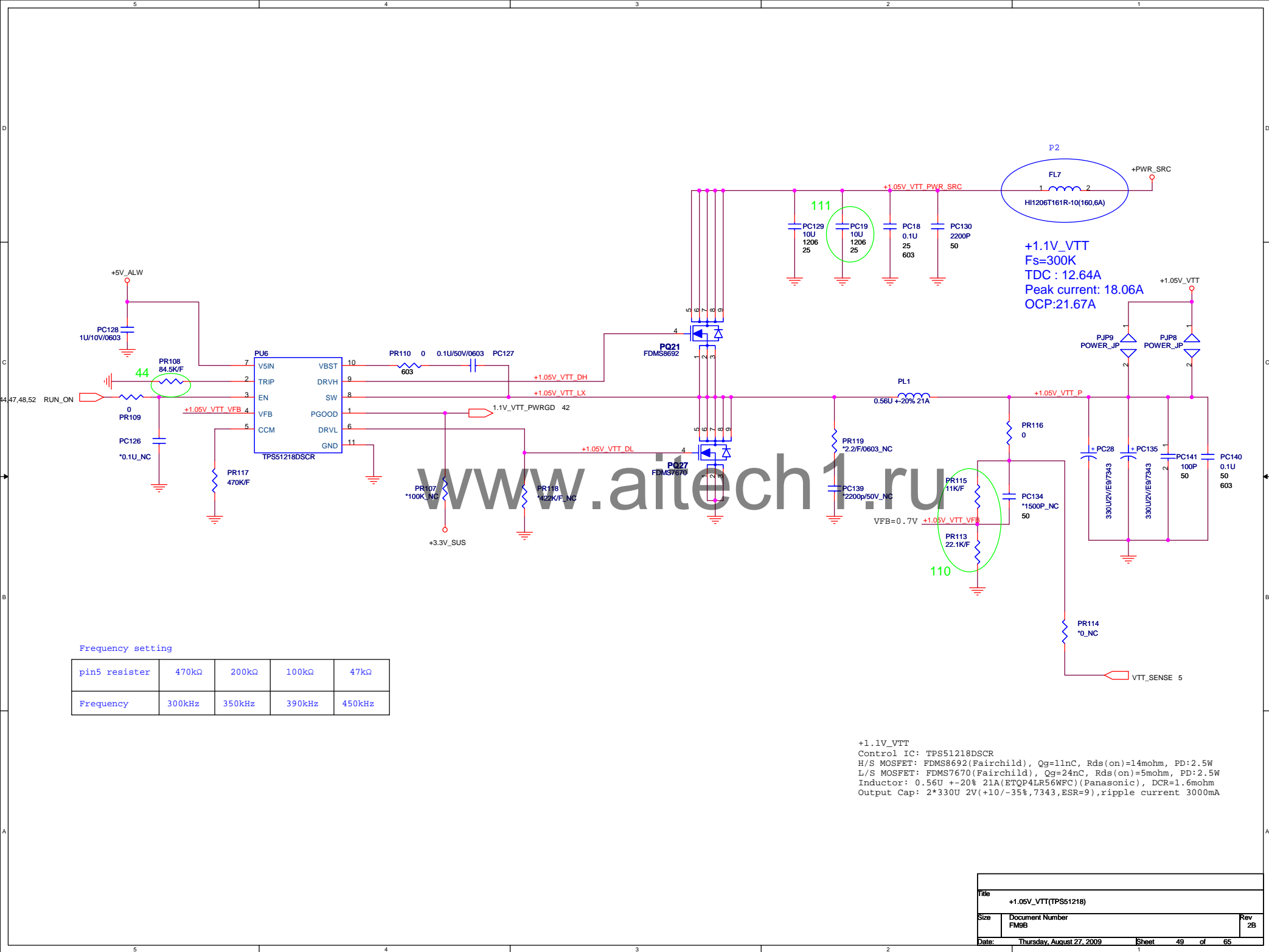
Size  
Document Number  
FM9B

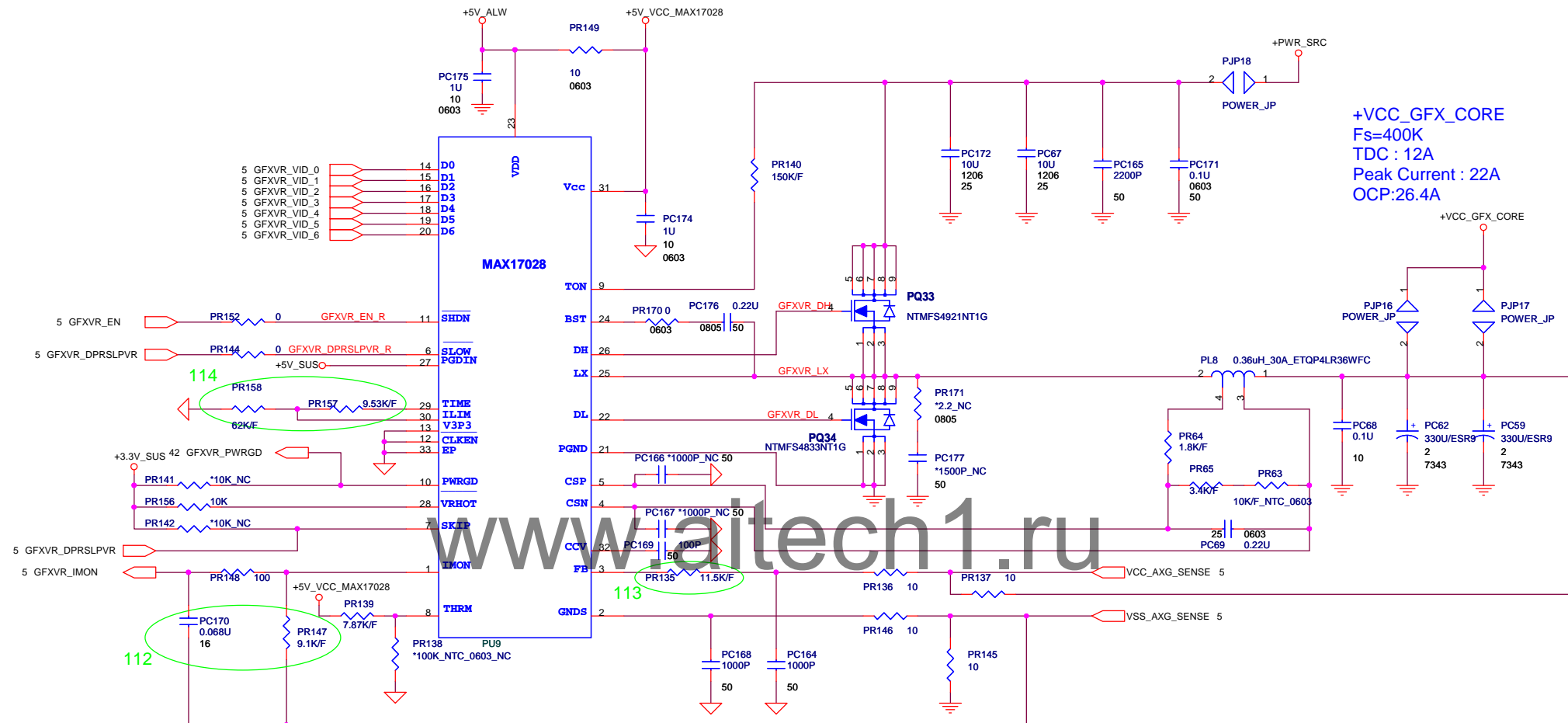
Rev  
2B

Date: Thursday, August 20, 2009 Sheet 46 of 65





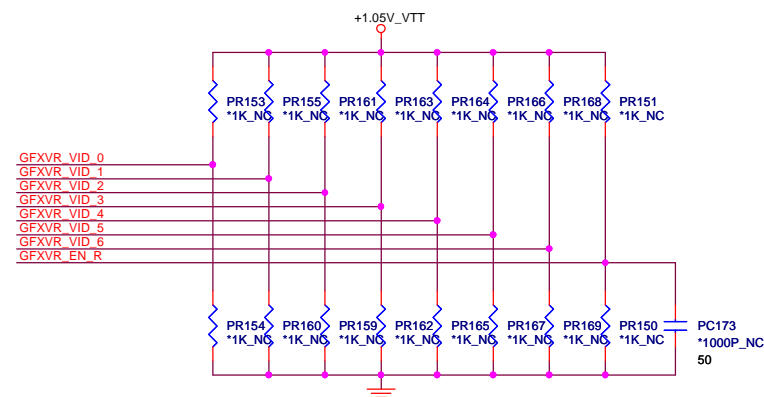
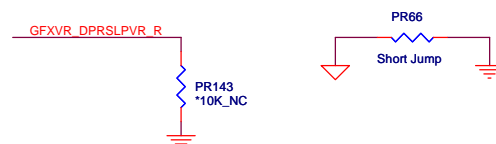




+VCC\_GFX\_CORE  
Fs=400K  
TDC : 12A  
Peak Current : 22A  
OCP:26.4A

112

113

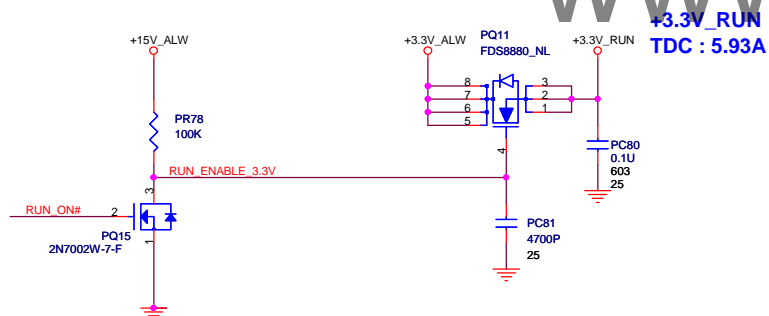
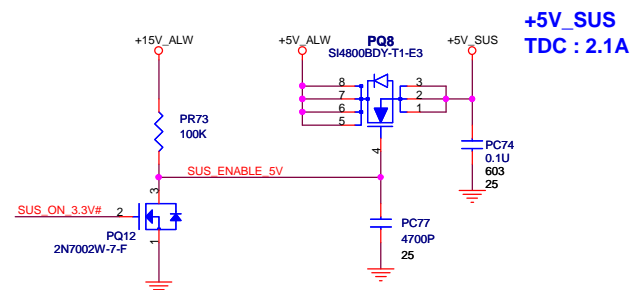
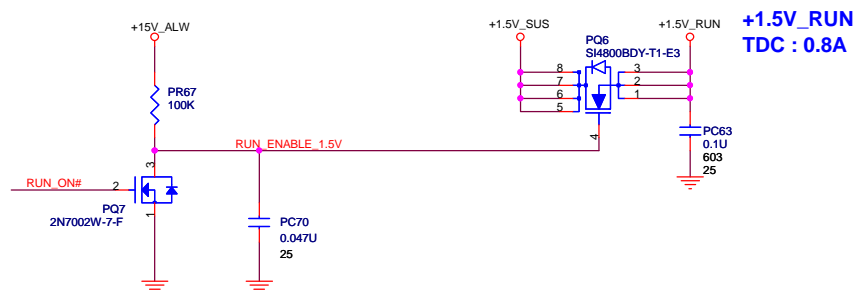
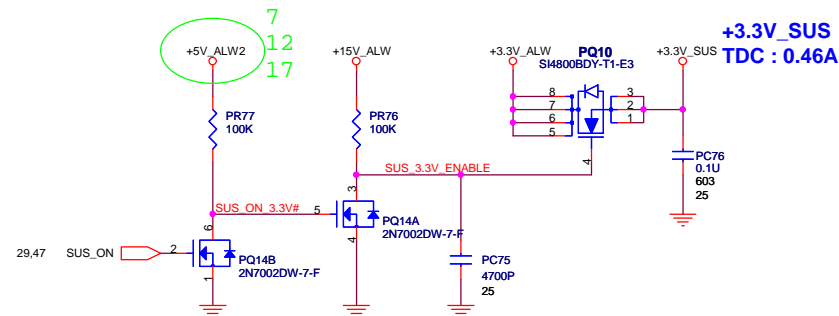
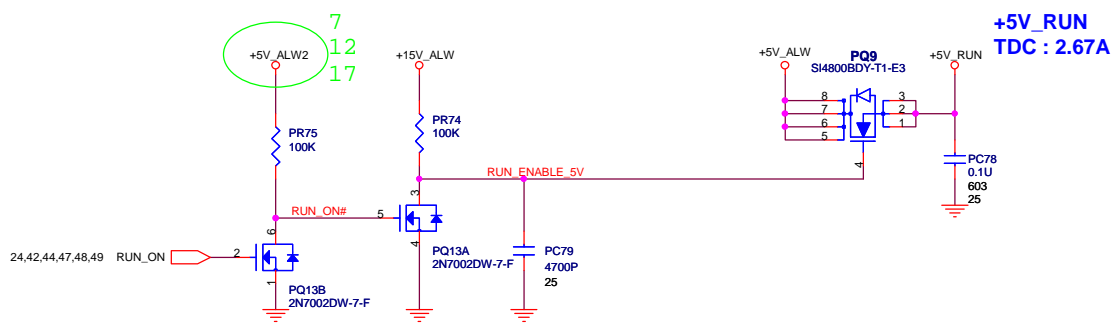


Default Vcc\_Core voltage is 1.0500V

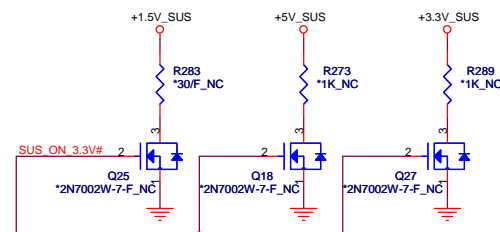
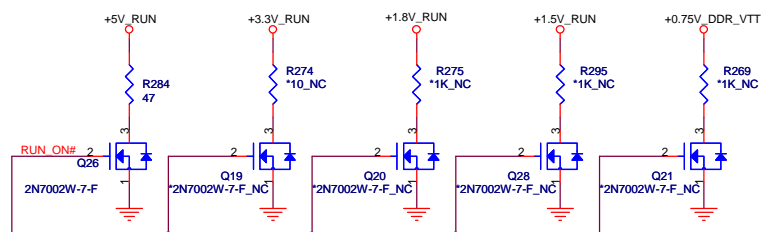
QUANTA  
COMPUTER

Title VGA DC/DC		
Size FM9B	Document Number	Rev 2B
Date: Thursday, August 27, 2009	Sheet 50	of 65

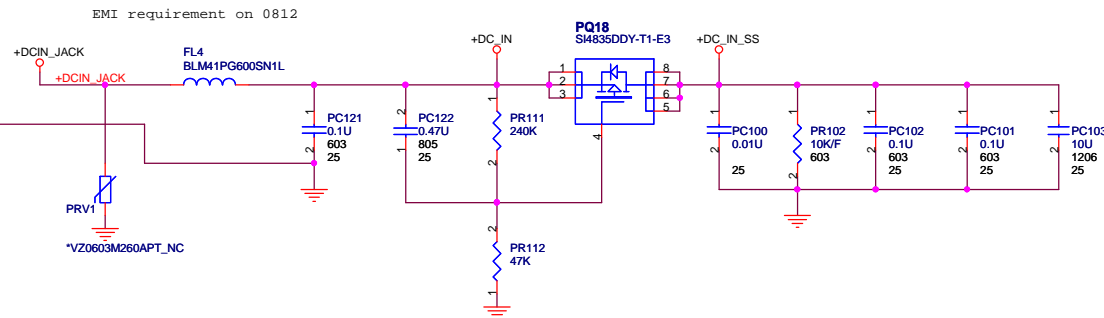
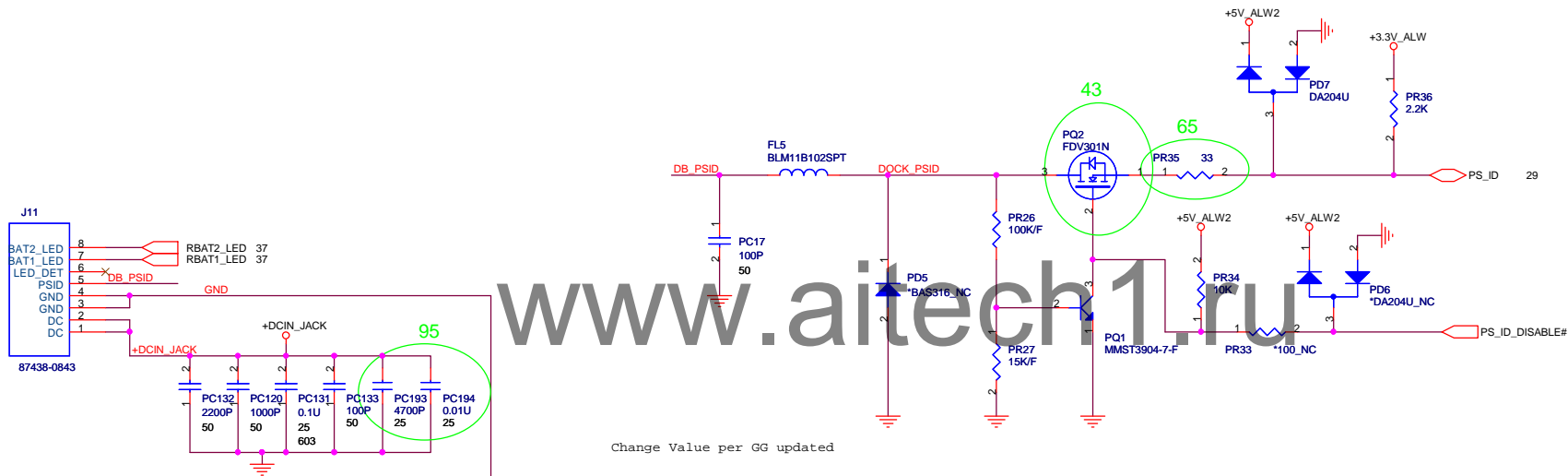
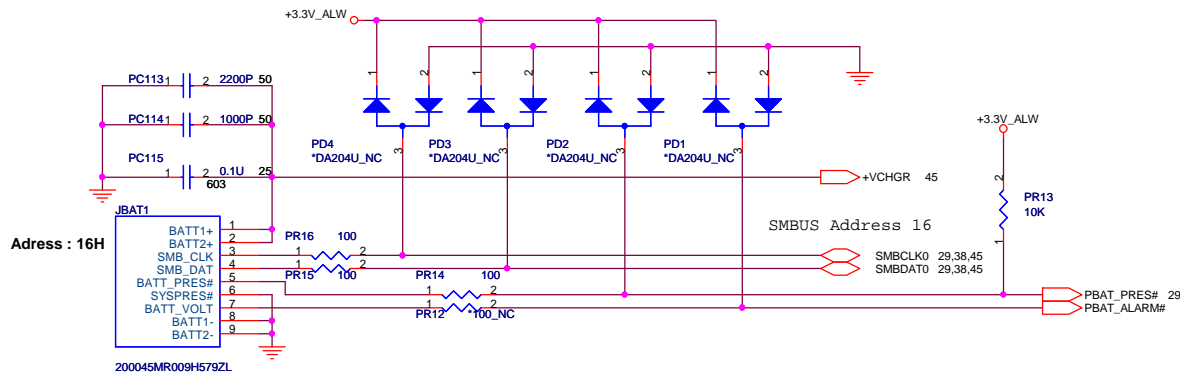




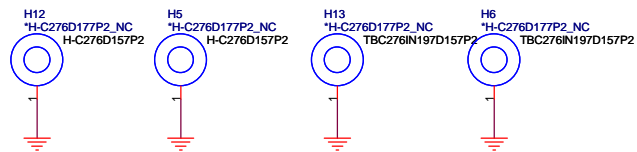
### Reserve discharge path



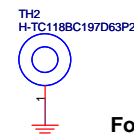
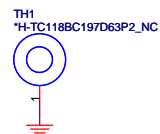
Title		
RUN / SUS POWER SW		
Size	Document Number	Rev
FM9B		2B
Date:	Thursday, August 20, 2009	Sheet 52 of 65



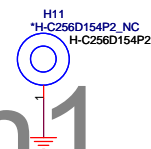
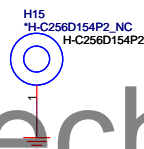
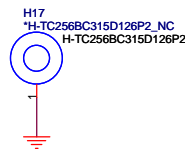
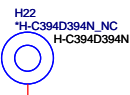
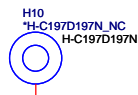
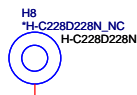
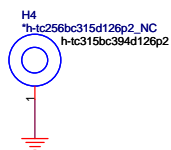
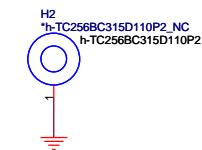
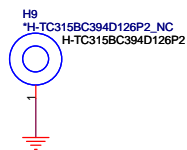
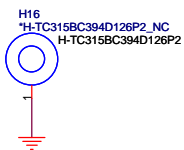
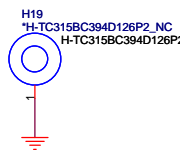
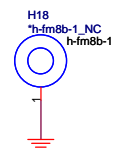
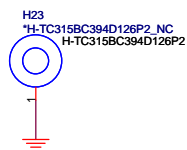
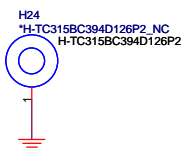
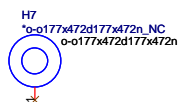
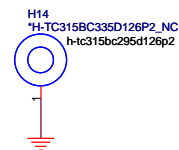
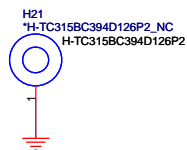
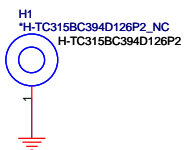
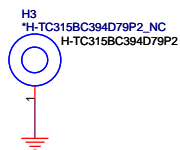
# FOR CPU use



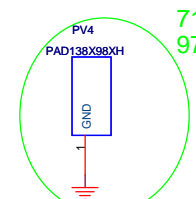
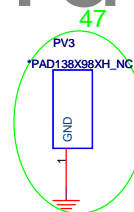
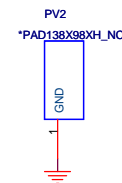
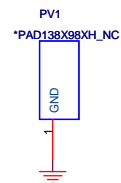
87



For MiniCard nut use.  
on 31' header



For PCH nut use.



47

71  
97


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Title SCREW PAD		
Size FM9B	Document Number FM9B	Rev 2B
Date: Tuesday, August 25, 2009	Sheet 54	of 65

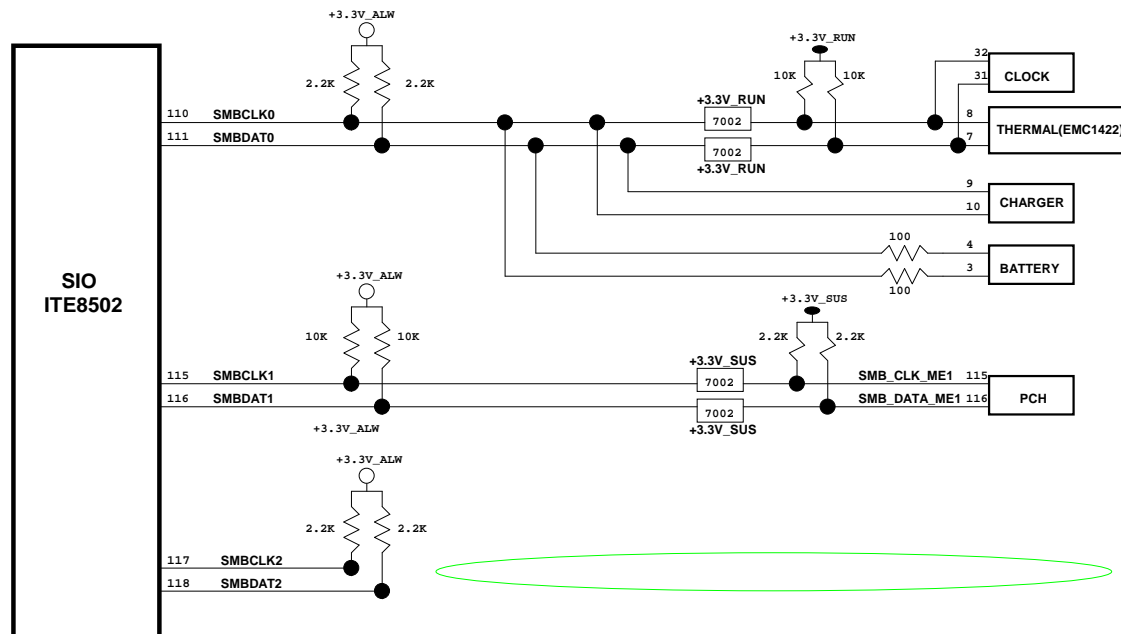
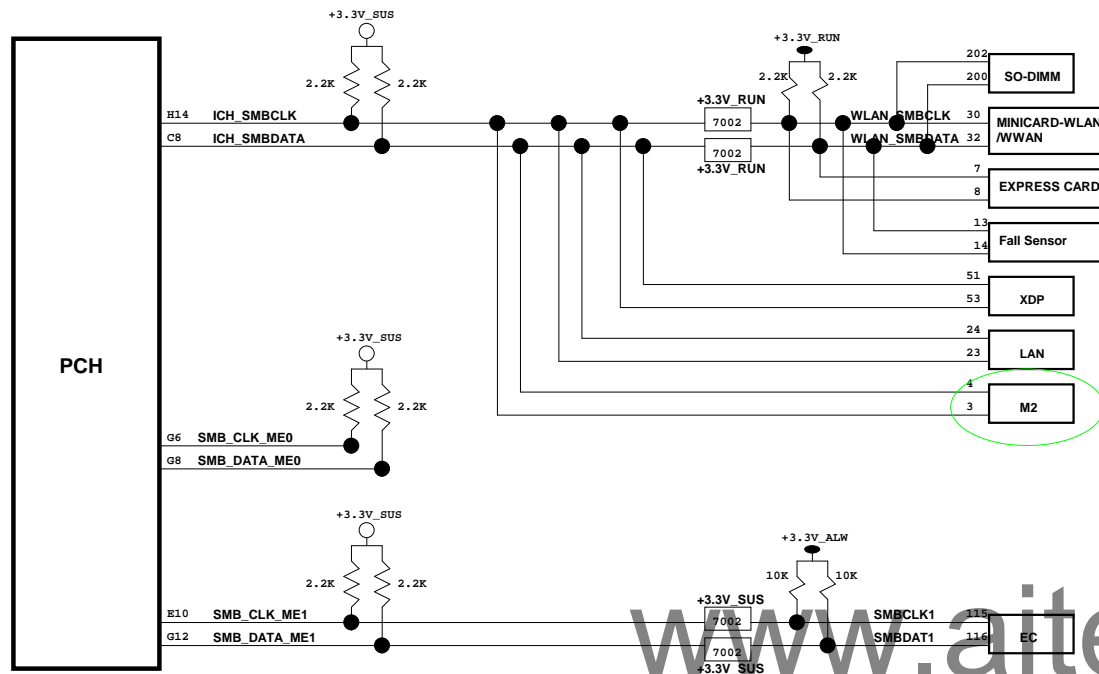
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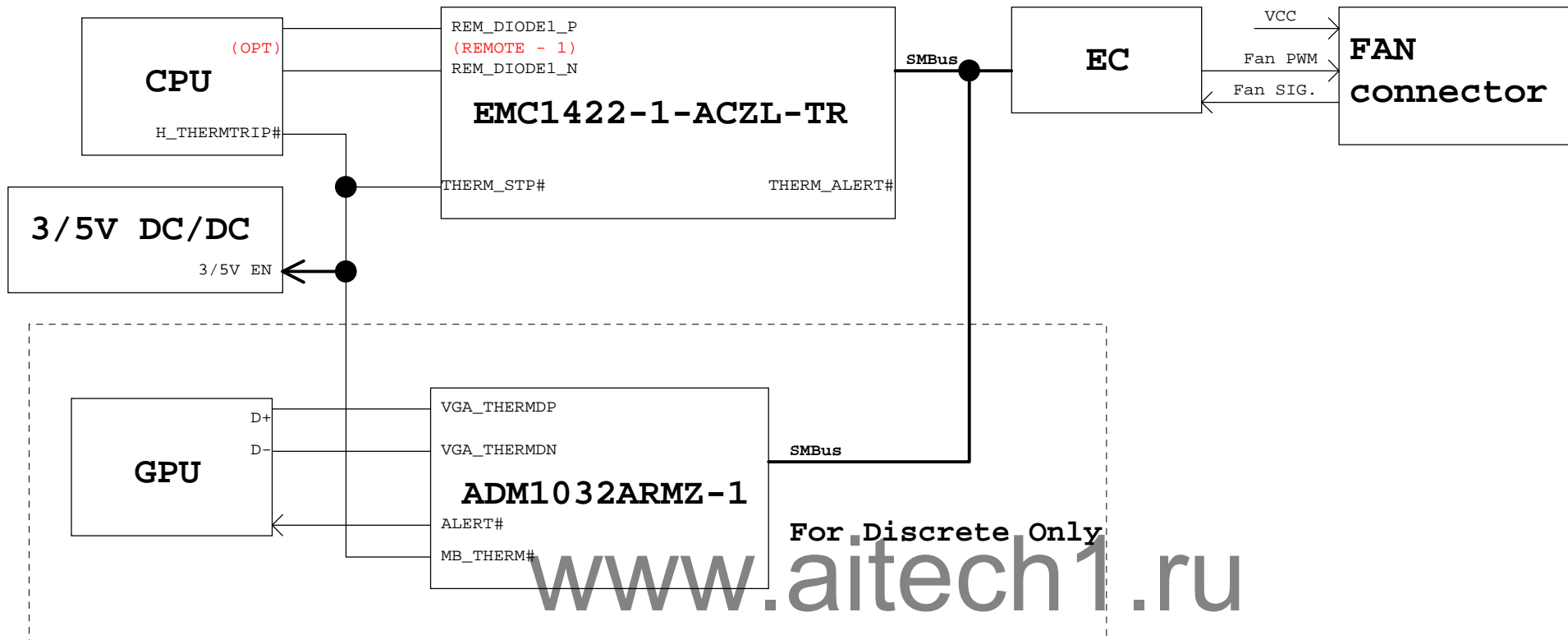
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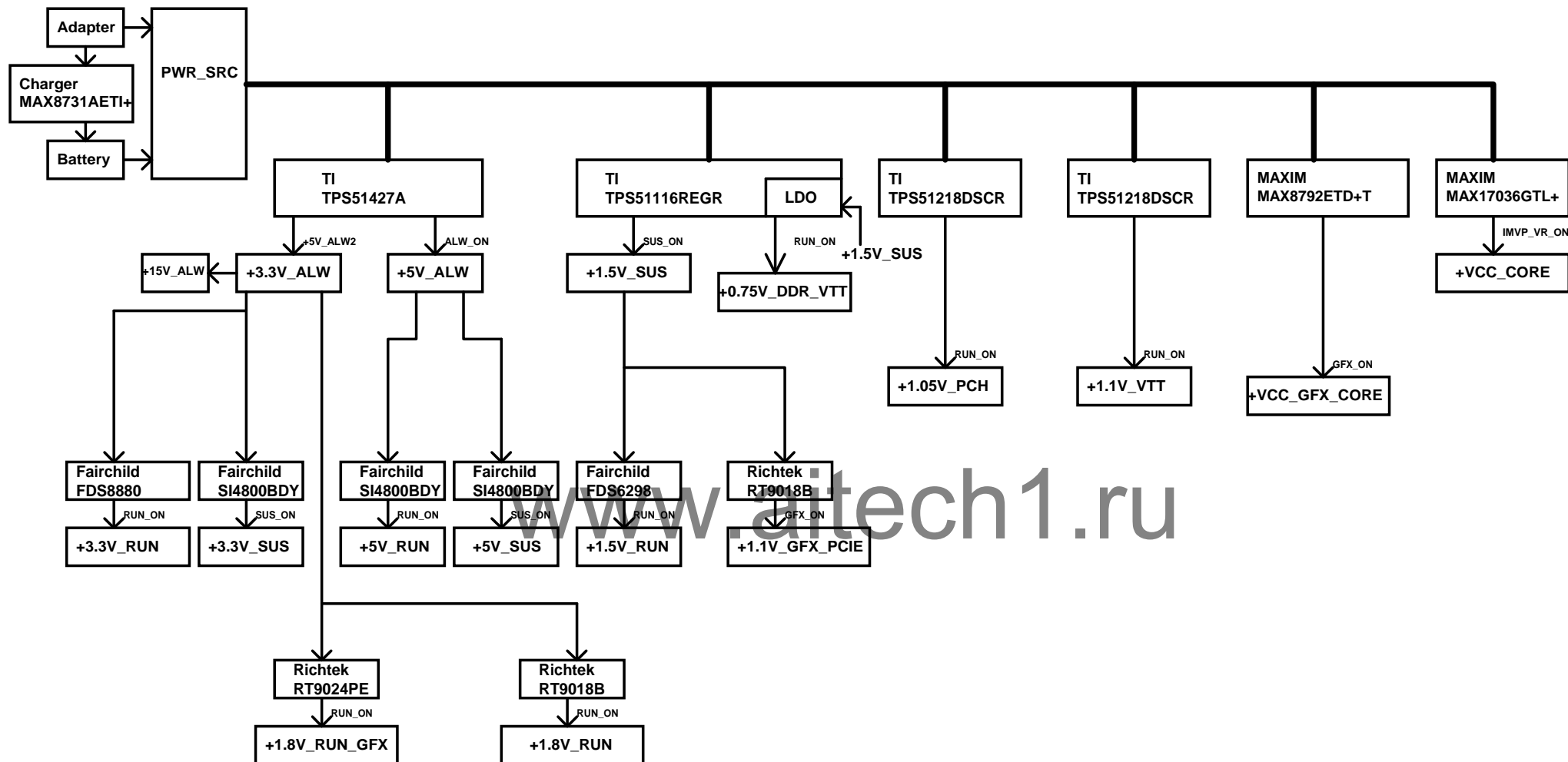


QUANTA  
COMPUTER

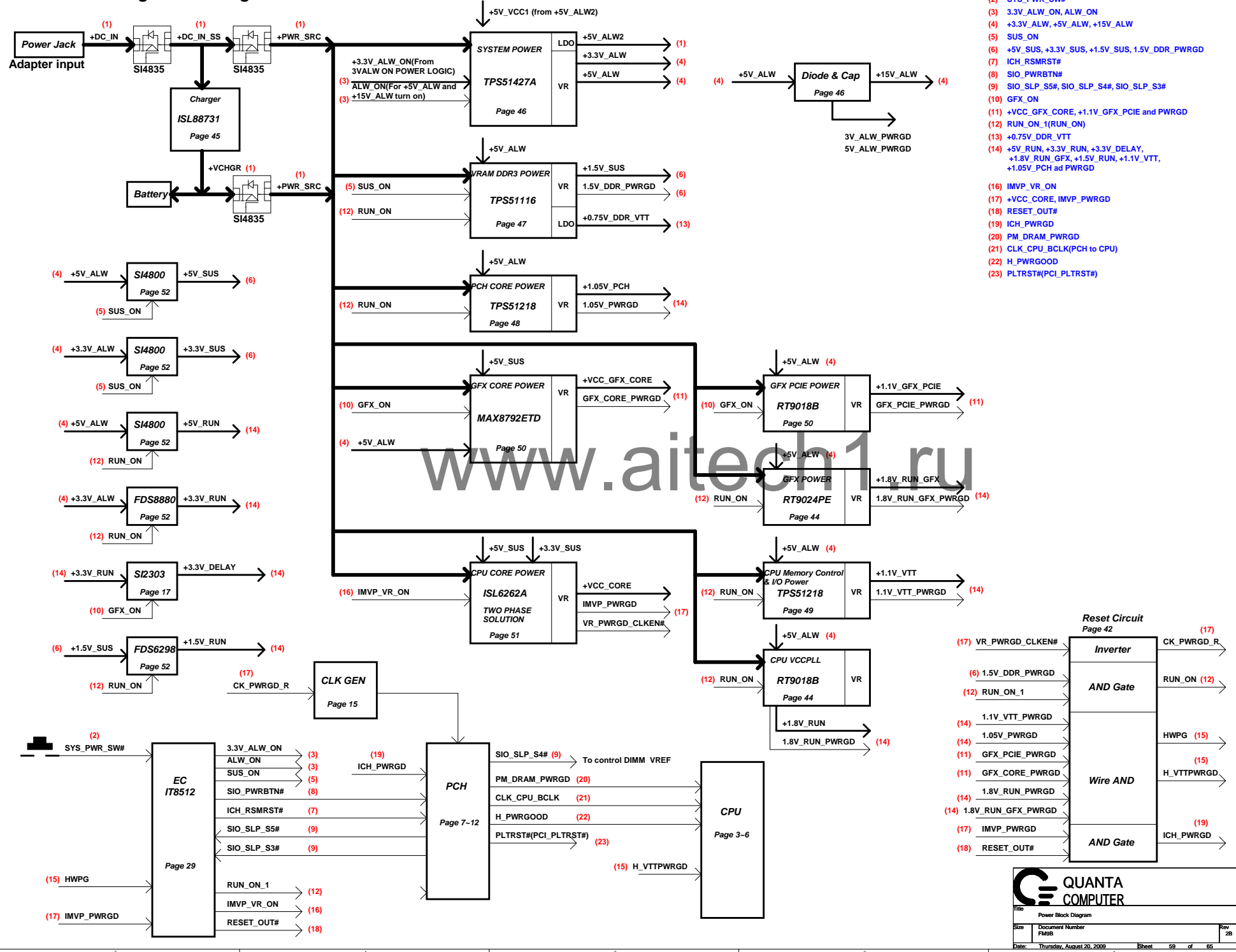
Title		
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Size	Document Number	Rev
FM9B		2B
Date:	Thursday, August 20, 2009	Sheet 55 of 65

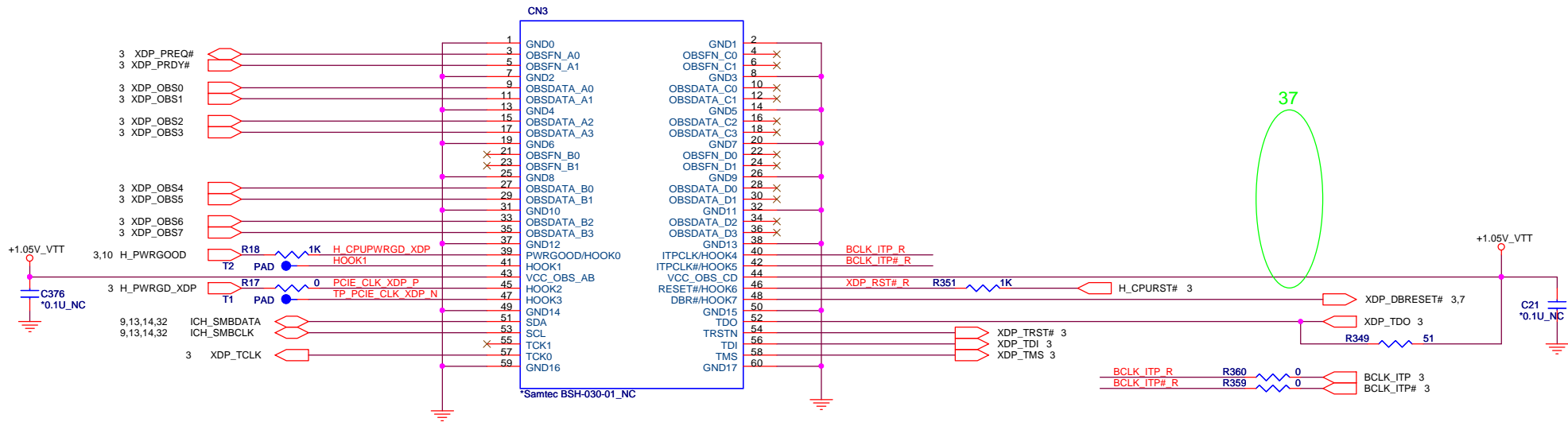







# FM9 Power Design Block Diagram 2009/02/25





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 <b>QUANTA COMPUTER</b>		Title	
		SMBUS BLOCK	
Size	Document Number	Rev	
	FM98	2B	
Date:	Thursday, August 20, 2009	Sheet	60 of 65